72-1018-A

Instruction Manual

Vikings

MODEL 5845

MULTI FUNCTION COUNTER
8 DIGIT/
150 MHz

DATA PRECISION

Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_08019

72-1018

Instruction Manual

MODEL 5845

MULTI FUNCTION COUNTER
8 DIGIT/
150 MHz

First Edition October, 1980
Copyright 1980, Data Precision Corporation
Printed in U.S.A.

PROPRIETARY NOTICE

The information contained in this publication is derived in part from proprietary and patent data of the Data Precision Corporation. This information has been prepared for the express purpose of assisting operating and maintenance personnel in the efficient use of the instrument described herein, and publication of this information does not convey any rights to reproduce it or to use it for any purpose other than in connection with the installation, operation, and maintenance of the equipment described herein.

CONTENTS

1. INTRODUCTION

1.1 General Description
1.2 Features
1.3 Accessories and Options

2. SPECIFICATIONS

2.1 Frequency Measurement
2.2 Period Measurements
2.3 Events Measurement
2.4 Seconds Measurement
2.5 Instrument Performance
    2.5.1 Time Base
    2.5.2 Input Characteristics
    2.5.3 Display
    2.5.4 Power, Physical, Environmental
    2.5.5 Options

3. OPERATION & RECALIBRATION

3.1 General
3.2 Unpacking & Repacking
3.3 Front Panel Features
3.4 Rear Panel Features
3.5 Operating Procedures
    3.5.1 Scope
    3.5.2 Input Connections and Setup Hints
    3.5.3 Measuring Frequency
    3.5.4 Measurement of Period (Interval)
    3.5.5 Counting Events
    3.5.6 Measuring Lapsed Time
3.6 BCD I/O Option
    3.6.1 Operating Modes
    3.6.2 External Time Base
    3.6.3 Remote Status/Control Setup
    3.6.4 BCD Data
    3.6.5 Function and Range

3.7 Recalibration Procedure
3.7.1 General
3.7.2 Procedure (Standard Time Base)
3.7.3 Procedure (TCXO Option)

4. PRINCIPLES OF OPERATION

4.1 System Block Diagram
4.2 Input Signal Conditioner
4.3 Programmable Time Base
4.4 Gate and Intercycle Control
4.5 8-Decade Counter & Display
4.6 Hold and Reset Functions
4.7 Function and Range Select Switches
4.8 Power Supply
4.8.1 Regulated and Unregulated Supplies
4.8.2 Power-Up Resetting
4.9 I/O Option
4.9.1 General
4.9.2 BCD Outputs
4.9.3 Print Enable, Start, and Stop

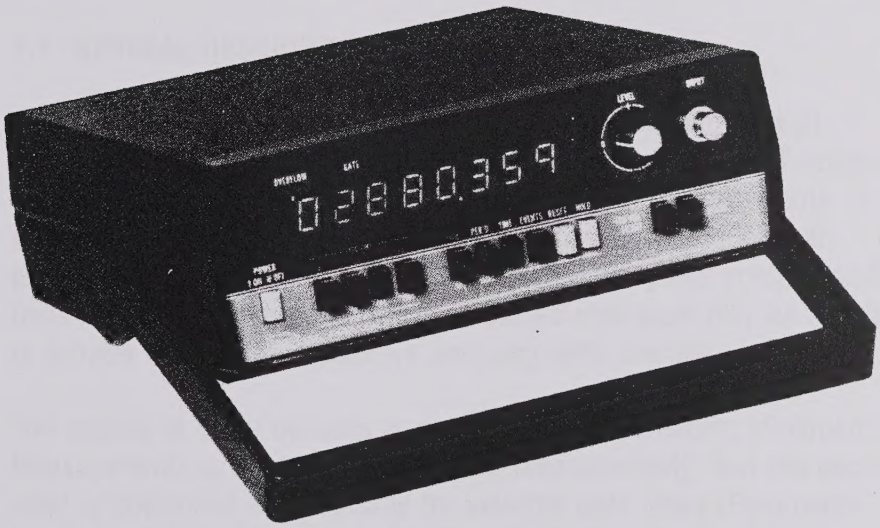
5. MAINTENANCE

5.1 General
5.2 Troubleshooting Strategy
5.3 Test Points

6. PARTS LISTS

6.1 General
6.2 Standard Model Parts List (Including TCXO Option)
6.3 I/O Option Board Parts List

7. REFERENCE DRAWINGS



Frontispiece. Model 5845 8 Digit/150MHz Multifunction Counter

1
INTRODUCTION

1.1 GENERAL DESCRIPTION

Data Precision's Model 5845 is a complete multifunction, 8-digit, 150 MHz counter/timer. Its standard configuration provides Frequency, Period, Period Average, Events, and Time Interval measurements. A single I/O Option board provides the capability for introducing an external clock frequency, as well as remote display and control connections. An optional temperature compensated time base may be installed to achieve improved temperature and long-term stability.

The display of 8 full decades is direct reading in kilohertz (Frequency Measurement) or microseconds (Period Measurement), and the decimal point is positioned automatically for selected gate times (Frequency Measurement) and for a selected number of periods averaged (Period Measurement). Time Measurement is directly in seconds with resolution in milliseconds (three decimals).

1.2 FEATURES

- Big, Bright 0.43" LED Display.
- Frequency:
  Sinewave: 5 Hz to 150 MHz;
  Pulse: 0 to 1.5×10^8 pps.
- Single Period: 0.5 to 200,000 μsec.
- Period Average: 10, 100, 1000 periods.
- Totalizing (Event Counting): 0 to 9,999,999 (counting continued after overflow) with pulse-pair resolution of 15 nsec.
- Seconds Measurement: 0 to 99,999.999 seconds (27.78 hrs.)
- Sensitivity: 10 mV RMS over wide frequency range
- Accuracy: Time-base accuracy ±1 count.
- Stability: ±0.01 ppm/sec, ±0.6 ppm/month, ±4.0 ppm/year.
- Resolution: 100 Hz with 0.01 sec gate time through 0.1 Hz with 10 sec gate time in four-decade increments.
- Line Powered: 100/115/230 volts, 47–400 Hz (internal selection).

1.3 ACCESSORIES AND OPTIONS

C7.	BCD data with Mode, Range, Print and Overflow outputs. Accepts Hold, Reset, Start/Stop, Mode and Range command inputs. Accepts external 10 MHz clock input.
AN10A.	Whip Antenna
BN85.	Test Cable (5' BNC to BNC)
C4.	50Ω Input Termination
T1.	Test Probe (4' BNC-to-2 mm probe)
TB9.	Precision Time-Base Crystal Oscillator
CC50.	Carrying Case

2

SPECIFICATIONS

2.1 FREQUENCY MEASUREMENT

Input:

Sinewave: 5 Hz to 150 MHz
Pulse: 0 pps to 150,000,000 pps
Double pulse resolution: 15 nsec

Gate Time/Resolution:

0.01 sec/100 Hz
0.1 sec/10 Hz
1.0 sec/1 Hz
10 sec/0.1 Hz

Accuracy:

Time base accuracy ± 1 count

Readout:

Directly in kilohertz (8 digits)

2.2 PERIOD MEASUREMENTS

Input:

Sinewave: 0.5 to 200,000 μs (5 Hz–2 MHz)
Pulse: 0.5 to 99,999,999 μs (0 pps to 2,000,000 pps)

Periods Averaged/ Resolution;

1/1 μs
10/0.1 μs
100/0.01 μs
1000/0.001 μs

Accuracy:

Time base accuracy ± 1 count

Readout:

Directly in microseconds

2.3 EVENTS MEASUREMENT

Input:

Sinewave: 5 Hz to 2 MHz
Pulse: 0 to 2,000,000 pps

Display Range:

0 to 99,999,999
Counting continues after overflow

2.4 SECONDS MEASUREMENT

Display Range:

0 to 99,999.999 seconds (27.78 hours)
Counting continues after overflow.

2.5 INSTRUMENT PERFORMANCE

2.5.1 Time Base:

Type:

High stability crystal

Frequency:

10 MHz

Accuracy:

±0.01 ppm/sec
±0.6 ppm/month
±4.0 ppm/yr

Temperature:

±5 ppm, from 0°C to 40°C

Warmup Time:

30 minutes to rated performance

2.5.2 Input Characteristics

Coupling:

Ac (RC time constant approximately 0.05 seconds)

Impedance:

@ x20 ATTEN: 1 MΩ || 25 pF
@ x1 ATTEN: 1 MΩ || 25 pF for Vin < 1 V.
66 KΩ for Vin >1 V.

Sensitivity (x1 Attenuation):

Sinewave: 10 mV rms, 5 Hz to 20 MHz
Linearly to 50 mV @ 150 MHz
Pulse: 30 mV p-p for 25 ns width
Linearly to 150 mV p-p for 7.5 ns width

Trigger Level:

Adjustment range
@ x1 Atten: = ± 0.25 V
@ x20 Atten: = ± 5 V

Filter:

Switchable low-pass filter, 100 kHz pass band

Maximum Input w/o Damage:

Sinewave: Dc to 50 kHz: 250 V rms
50 kHz to 2.5 MHz: 1.25 x 10^7 Volt x Hertz
2.5 MHz to 150 MHz: 5 V rms

2.5.3 Display

8 LED decimal digits (0.43" high)
5 LED decimal points (automatically positioned)
2 LED Annunciators (**GATE**, **OVERFLOW**)

2.5.4 Power, Physical, Environmental

Power:

105 to 125 V, 210 to 250 V, or 90 to 110 V
47 to 400 Hz
Factory connected
12 watts, maximum

Package:

Plastic Case
2-7/8" x 8-1/2" x 8-7/8"
Weight: 4 lbs.

Operating Temperature:

0 °C to 40 °C

Storage Temperature:

−25 °C to +75 °C

Humidity:

0 to 80% RH, non-condensing

2.5.5 Options

Temperature compensated time base (TCXO)

Stability vs Time: ± 1 ppm/year
Stability vs. temperature: 2 ppm max deviation over range from 0°C to 40°C.

Input/Output Option

BCD Output: 8 digits, Print Enable, Overflow, 4 Output Disable
Remote Start/Stop: Start, $\overline{\text{Stop}}$, $\overline{\text{Reset}}$
Mode Programmable
Range Programmable

All inputs and outputs are compatible with 5-volt CMOS or LS-TTL circuits, except the range and mode signals that are compatible with 5-volt CMOS only.

BCD outputs are 3-state and will drive 1 TTL load.

External Clock (10 MHz):

Input Sensitivity: 300 mV p-p minimum
Maximum Input Voltage: 5 V p-p

3
OPERATION
&
RECALIBRATION

NOTE: Read this chapter carefully before attempting to use your Model 5845 Counter. Retain these instructions. Observe all WARNINGS and CAUTIONS.

3.1 GENERAL

Chapter 3 contains detailed instructions for connecting and operating the Model 5845 Counter. Refer to the specifications in Chapter 2 to obtain the tolerance with which displayed measurements may be interpreted, and to determine the limitations on the input signal within which the specified performance of the counter is applicable.

The rear panel mounts a standard grounding lug, electrically connected to the ''ground'' terminal of the 3-wire line cord receptacle in the rear panel. Make a good earth connection.

3.2 UNPACKING & REPACKING

a. Figure 3-1 identifies the components of the packaging configuration for Model 5845 Counter. As shown in that illustration, the Counter is placed in a waterproof plastic wrapper, securely fitted between molded-foam shock isolators, and placed with the documentation in its shipping carton. When unpacked, you should find:

(1) Model 5845 Counter
(2) Packing Slip
(3) Certificate of Conformance
(4) Warranty Card
(5) Factory Test Data Sheet
(6) Spare 2/10 A, 3AG, Slo-Blo Fuse

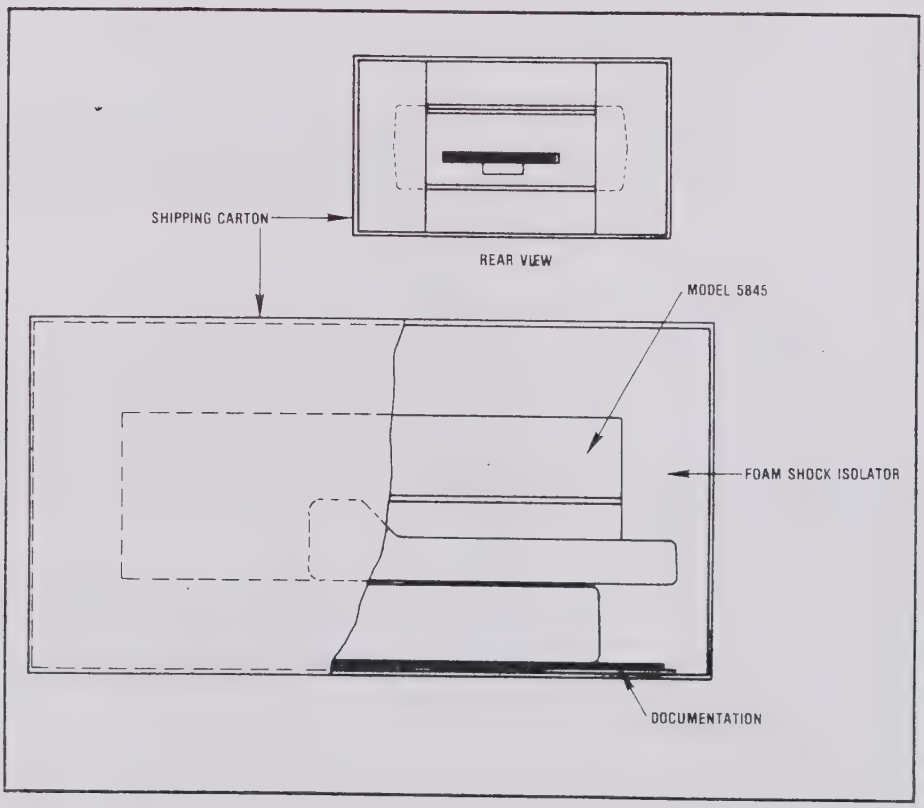


Figure 3-1. Shipping Configuration

b. Carefully examine these articles, noting especially the matching serial numbers of the instrument and the test data. Inspect the packing case and the instrument for any signs of damage during shipment and report immediately to the carrier. Fill out and return the warranty card to register your instrument and to establish your warranty service interval.

c. Accessories, such as coaxial input connectors, mating I/O connector, input antennas, etc., may have been ordered. These will be shipped in their own containers.

If the TCXO Option (Temperature-compensated, ultra-stable time base) has been ordered, it will be installed in the Counter.

If the I/O Option has been ordered, it will be installed in the Counter.

d. Retain the packing material for reshipment. When shipping Model 5845, place the instrument in its protective carrying case. Use foam liners and pack in original shipping carton, if available. If original foam packing is not available, use some form of shock insulation material, such as bubble plastic, and pack the instrument for maximum protection against shock during transit.

3.3 FRONT PANEL FEATURES

Figure 3-2 illustrates the controls and indicators of the Model 5845 front panel, and Table 3-1 contains a brief description of the features of each.

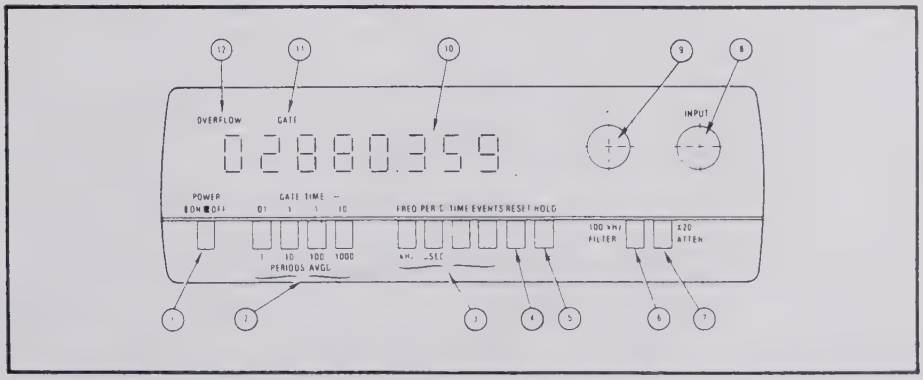


Figure 3-2. Front Panel

Table 3-1
FRONT PANEL FEATURES
(See Figure 3-2)

Item	NAME*	Description/Function
1	POWER ON OFF	Push-push switch. Applies or removes ac power to Counter power supply circuits
2	GATE TIME PERIODS AVGD	Four interlocked pushbuttons. Selects GATE TIME when in Frequency Measurement, or Number of PERIODS AVERAGED when in Period Measurement. All four buttons must be in released position when exercising this selection from a remote location via I/O Option.
3	FREQ PER'D TIME EVENTS	Four interlocked pushbuttons. Selects Counter Measurement function. All four buttons must be released when exercising this selection from a remote location via I/O Option.
4	RESET	Momentary-contact pushbutton. When actuated, resets the Counter to zero.
5	HOLD	Push-push switch. When in depressed position, value in display is retained and count is stopped. Count resumes when switch is released. Normally used in EVENTS and TIME measurements. Must be placed in released position if this function is to be exercised from a remote station via the I/O Option.
6	100 kHz FILTER	Push-push switch. When in depressed position, a 100 kHz filter is inserted in the input signal conditioning circuit.
7	x20 ATTEN	Push-push switch. When in depressed position, input signal is attenuated by a factor of 20.
8	INPUT	BNC Coaxial connector for input signal to be measured.
9	LEVEL	Potentiometer. Adjusts trigger level (± 0.25 V) for input signal threshold.
10	Display	8 decades of 7-segment LED digits. Automatic positioning of decimal point for direct reading in kHz (Frequency Measurement), or microseconds (Period Measurement), or milliseconds (Time Measurement).

Table 3-1 (Cont.)

Item	NAME*	Description/Function
11	GATE	LED annunciator. Lighted when internal counter is gated for a measurement.
12	OVERFLOW	LED annunciator. Lighted when count exceeds 99 999 999. (Counter continues to count, unless stopped, and display is excess beyond 100 000 000.)

* All capital letters indicates an exact spelling as on the front panel. Upper and lower case used to identify other item.

3.4 REAR PANEL FEATURES

Figure 3-3 illustrates the rear panel of the Model 5845, and Table 3-2 contains a brief description of the features of each of the controls and connectors mounted in the panel.

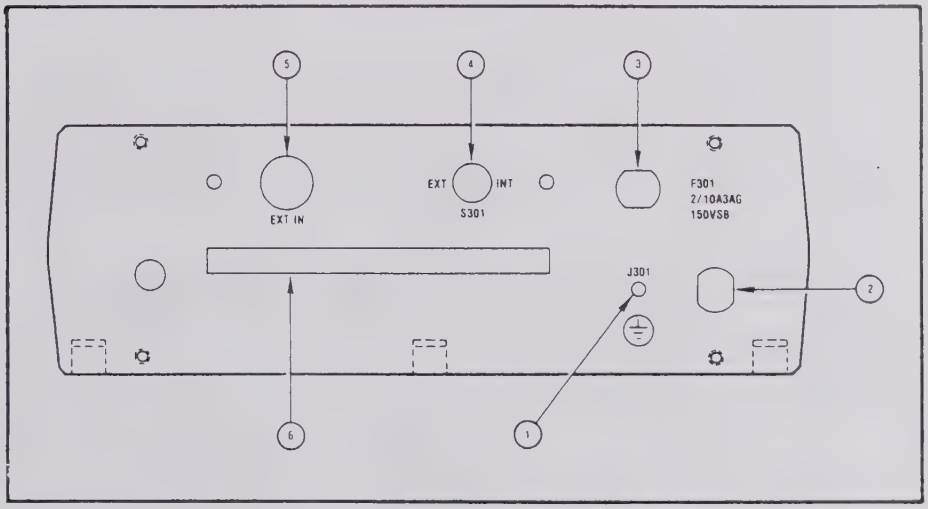


Figure 3-3. Rear Panel

Table 3-2
REAR PANEL FEATURES
(See Figure 3-3)

Item*	NAME**	Description/Function
1	J301	Ground lug. For connecting to earth ground.
2	Line Cord	Connected 3-wire line cord. Center conductor internally connected to ground lug J301.
3	F301	3AG Fuse. 2/10 A, 250 V, Slo-Blo.
4*	EXT - INT S301	Single-pole double-throw switch. In EXT position, connects rear panel time base counter signal to counter circuitry.
5*	EXT IN	BNC coaxial connector, to connect external time base to Model 5845.
6*	PC-Board Edge Connector J202	Connector for I/O status and control signals.

*Indicates that this item is available only when the I/O Option has been installed.
**All capital letters are used to indicate the exact form as it appears on the rear panel. Upper and lower case letters are used otherwise.

3.5 OPERATING PROCEDURES

3.5.1 Scope

This paragraph contains step-by-step procedures for using the basic and option-enhanced Model 5845 to:

- Measure frequency of sinusoids and pulse trains (3.5.3)
- Measure period of sinusoids or between pulses (3.5.4)
- Count events (3.5.5)
- Measure lapsed time (3.5.6).

Paragraph 3.6 contains instructions for operation when the BCD I/O option is installed.

3.5.2 Input Connections and Setup Hints

Use BNC coaxial connector for the input signal. Data Precision accessories with mating BNC connector include:

- AN10A Whip Antenna, for measuring radiated signals;
- BN85 Test Cable, a 5-ft cable with BNC termination at each end, for long input lead requirements.
- T1 Test Probe, a short cable with 2-mm probe tip at one end.
- C4 50 Ω Termination, for impedance matching with 50 Ω conductors.

Assure good contact of connector with cable leads. Check connection at front-panel. The front panel connector outer shell is connected within the 5845 to earth ground. Observe caution in making any ground connections at the other end. Avoid ground loops.

If at all possible, monitor the input signal with a wideband oscilloscope. Check for noise, high frequency components, peak amplitude, and transients. Use **x20 ATTEN** control when input signal is larger than 5 volts. Use **100 kHz FILTER** when frequency of interest is less than 100 kHz.

In the subparagraphs that follow, the instructions are supported by illustrations of the front panel. For each counting function, a solid leader line is used in the illustration for a mandatory setting, and a dashed leader line is used for a setting where some judgment is used. The accompanying text describes the bases for making the variable settings.

3.5.3 Measuring Frequency (Fig. 3-4)

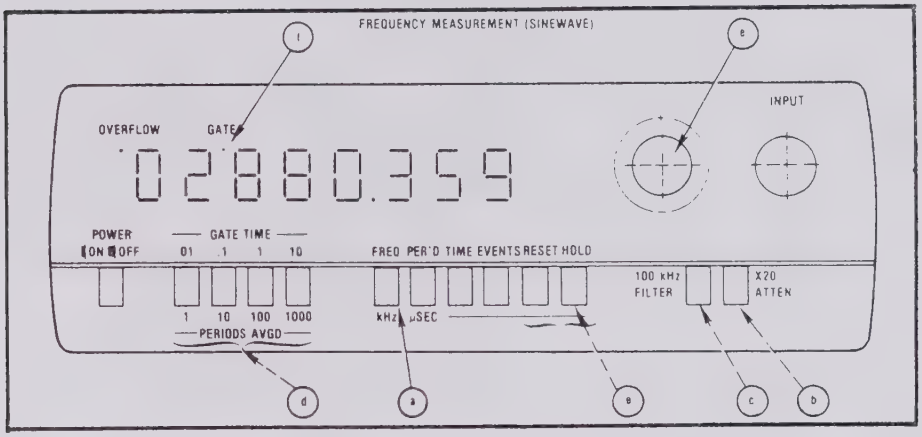


Figure 3-4. Frequency Measurement (Sinewave)

a. Select **FREQ** function.

b. Use attenuator if signal is greater than 5 V rms

c. Use filter if frequency of interest is less than 100 kHz.

d. Select **GATE TIME** to support application requirements for resolution, and throughput. If signal is noisy a longer gate time (within application requirements) is desirable. See table below.

GATE TIME (sec)	RESOLUTION (Hz)
0.01	100
0.1	10
1.0	1
10.0	0.1

e. For sinewaves, set Trigger Level at 0.
For pulse trains with low duty cycles, (positive or negative) see Figure 3-5. Adjust the Trigger Level accordingly,

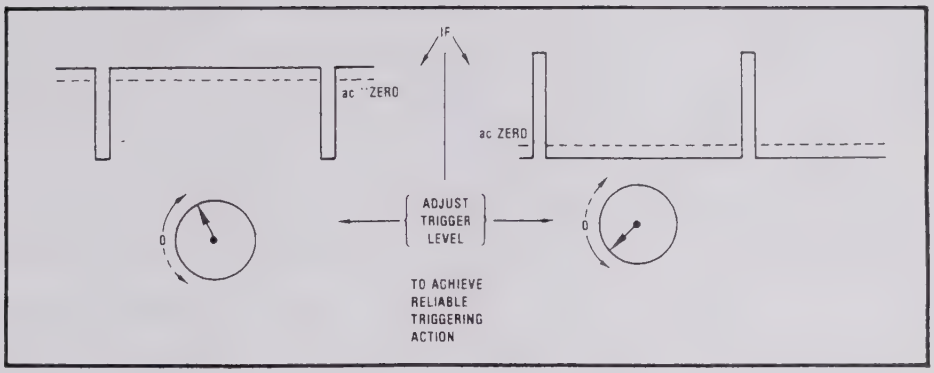


Figure 3-5. Trigger Level Adjustments for Low Duty Cycle Pulse Trains

f. Observe annunciator for gating operation. It should correspond with the selected gate time, and for the longer times the gating interval will be visually apparent.

g. Use **HOLD** and **RESET** pushbuttons when measurement is of signals that are intermittent, or bursts.

3.5.4 Measurement of Period (Interval) (Fig. 3-6)

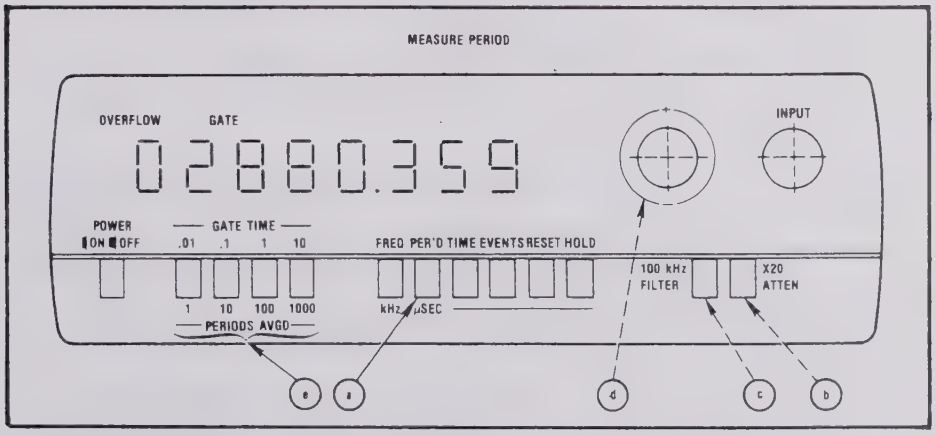


Figure 3-6. Measure Period

a. Operate the **PER'D** pushbutton.

b. Operate the attenuator if the signal is more than 5 volts rms.

c. Insert the 100 kHz filter if the interval corresponds to frequencies less than 100 kHz (more than 10 microseconds).

d. For sinewave inputs, set the trigger level to 0.
See Figure 3-4 and paragraph 3.5.3 for instructions on setting the trigger level when measuring pulse train intervals.

e. Select the number of **PERIODS AVG'D** according to the application requirements and the characteristics of the signal. See table below.

PERIODS AVG'D	RESOLUTION (μs)
1	1
10	0.1
100	0.01
1,000	0.001

Measurment is direct reading in microseconds. The decimal point is positioned automatically by the selection of the number of periods to be averaged.

3.5.5 Counting Events

Events to be counted should be transformed by external (to the 5845) circuitry to a voltage signal within the tolerances specified for measurement of pulse trains. Refer to the specifications in Chapter 2. Connect to the input.

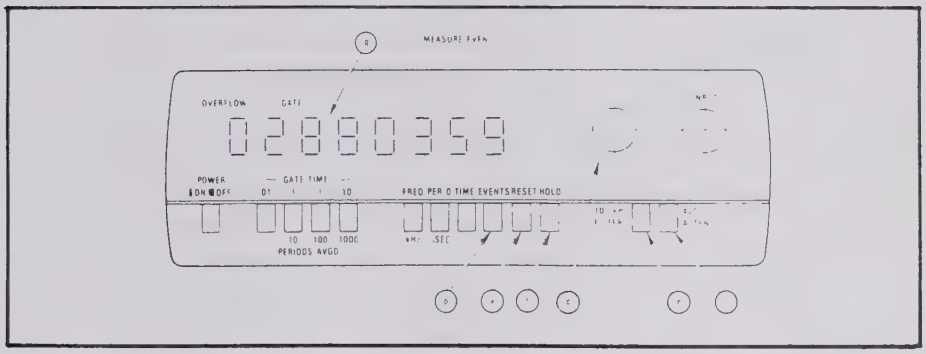


Figure 3-7. Measure Event

a. Operate the **EVENTS** pushbutton.

b. Insert the 100 kHz filter if frequency of information is less than 100 kHz.

c. Insert the x20 attenuator if the input voltage is greater than 5 volts.

d. Adjust the trigger level if the duty cycle is low. See Figure 3-4.

e. Keep **RESET** button depressed until start of counting interval. Release at the desired start of count.

f. Operate **HOLD** at end of count interval.

g. Read display directly in number of counts (no decimal point is lighted).

3.5.6 Measuring Lapsed Time

a. Operate **TIME** pushbutton.

b. Keep **RESET** button depressed until start of interval to be timed. Release at start of the interval.

c. Press **HOLD** button at end of interval.

d. Read display directly in seconds. Decimal point is positioned automatically so that display resolution is 1 millisecond.

3.6 BCD I/O OPTION

3.6.1 Operating Modes

When the BCD I/O option is installed, the counted value is available at the rear panel connector (J202) as latched parallel BCD values, with positive true logic, capable of driving 1 standard TTL or 5 V CMOS loads. Separate lines identify the selected range of the digital output. A status signal, **PRINT ENABLE** goes low for about 40 ms when the data is being updated in the latches, and its rising edge (after the data is stable) may be used to trigger remote printing. An **OVERFLOW** signal will identify counts above 99 999 999.

The **Range** and **Function** lines at the rear panel connector may be used for status information (output) or control operation (input). As output status signals, they are positive true logic, and can drive 5 V CMOS loads. As input control lines, they are driven by connecting to + 5 V.

When the BCD I/O option is installed, an external time base reference of 10 MHz or 1 MHz may be connected at the rear panel. If the 1 MHz input is used, then appropriate scaling of the displayed (remote) value is required.

3.6.2 External Time Base

a. Connect the external time base oscillator (1 or 10 MHz) to the rear panel input connector J203.

b. When an external time base is connected, either the internal or external time base may be used at any time. Operate the rear panel switch S301, **INT - EXT** to the appropriate position.

3.6.3 Remote Status/Control Setup

Prepare a cable with mating connector wired for the J202 terminal identification as shown in Table 3-3.

Table 3-3
MODEL 5845 REAR PANEL BCD I/O CONNECTOR (J202)

1	OVERFLOW	A	GROUND
2	RESET/	B	D8-8
3	STOP/	C	D7-1
4	START	D	D7-2
5	D8-2	E	D8-4
6	D8-1	F	D7-4
7	D6,5 DISABLE	H	D7-8
8	D6-8	J	GROUND
9	D6-4	K	GROUND
10	D5-1	L	GROUND
11	D5-4	M	D8,7 DISABLE
12	D4-8	N	D6-2
13	D4-4	P	D5-2
14	D4-2	R	D6-1
15	N.C.	S	D5-8
16	N.C.	T	D4-1
17	N.C.	U	D3-1
18	D3-2	V	D3-4
19	D3-8	W	D2,1 DISABLE
20	D4,3 DISABLE	X	D2-8
21	D2-4	Y	D2-2
22	D2-1	Z	D1-1
23	D1-2	a	D1-4
24	PRINT ENABLE	b	D1-8
25	PER'D	c	x1/0.01 sec
26	x10/0.1sec	d	EVENTS
27	TIME	e	x1000/10 sec
28	FREQ	f	x100/1 sec

3.6.4 BCD Data

The BCD values for the 8 digits are available as 32 separate lines (8 x 4) for use in parallel BCD configurations, or as selected groups of 8 lines for an 8-bit data bus configuration.

a. Parallel Output

To use the 32 lines for a parallel BCD output mode, jumper pins 7, 20, M, and W to digital ground, pin A.

b. Data Bus Output

BCD values for digits 1 and 2, 3 and 4, 5 and 6, 7 and 8 may be selectively connected as groups to an 8-bit data bus (4 x 2). This is accomplished by connecting the enable lines to ground for the respective digit pairs. The high level for these lines maintains a high impedance "decoupling" of the latched outputs for the lines not selected.

A typical connection block diagram is shown in Figure 3-8, in which the remote instrument selection of the digit address is decoded to activate the appropriate enable lines.

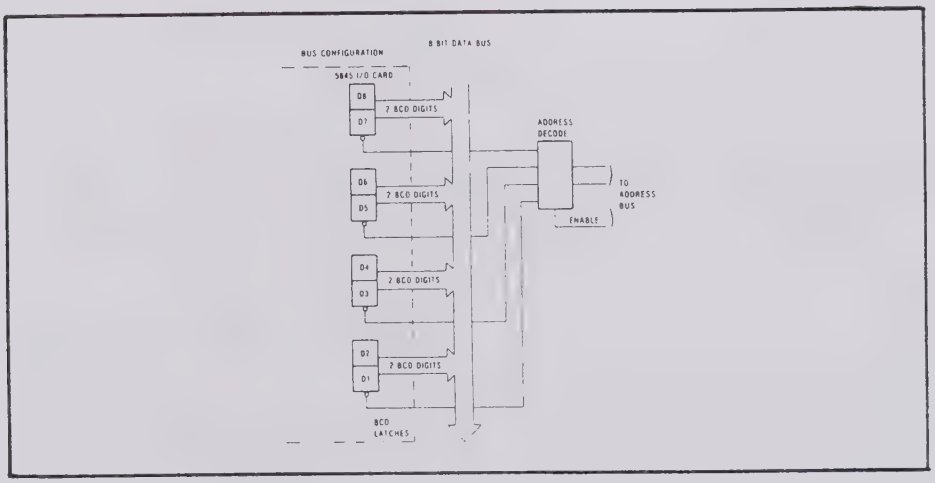


Figure 3-8. 8-Bit Data Bus Configuration

3.6.5 Function and Range

The function lines (**FREQ, PER'D, EVENTS, TIME**) and/or the range lines (**x1/0.01 sec, x10/0.1 sec, x100/1 sec, x1000/10 sec**) may be used as status or control independently in their respective groups. That is, function may be selected remotely while range is selected at the front panel; or range may be selected remotely while function is selected at the front panel; or both may be selected remotely; or both may be selected at the front panel.

When remote selection is desired, be sure that the front panel switches for that group are all operated to their released position.

3.7 RECALIBRATION PROCEDURE

3.7.1 General

The 5845 Counter requires only one recalibration adjustment. This control adjusts the time base frequency for precision measurements. A standard oscillator, with an accuracy of ±0.01 ppm or better at an output frequency from 10 MHz to 100 MHz, and an output amplitude up to 5 volts is required for the recalibration.

3.7.2 Procedure (Standard Time Base)

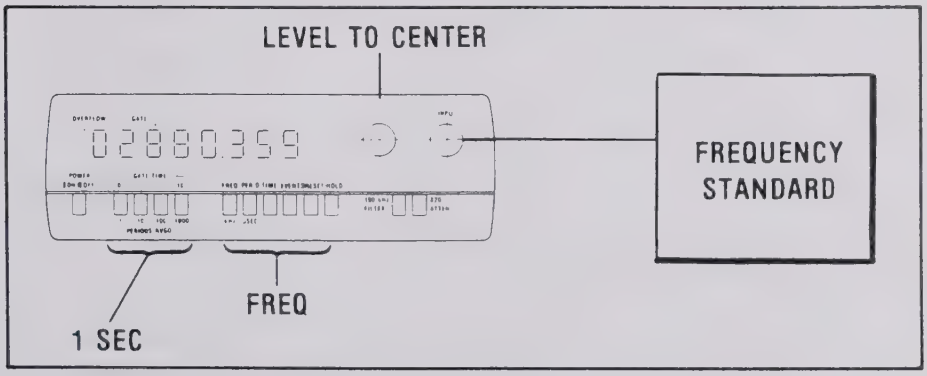


Figure 3-9. Recalibration Procedure

1. Allow a period of 30 minutes for the instrument to warm up with the cover in place.

2. Connect the frequency standard to the 5845 as shown in the illustration, Figure 3-9.

3. Set the 5845 to **FREQ** Mode, **1 sec GATE** Time, and **LEVEL** adjust to center (zero).

4. Remove the 5845 top cover.

5. Adjust C16 (Figure 3-10) until the 5845 displays the value set on the frequency standard.

   For a 100 MHz frequency input, the 5845 should display all zero's and the overflow annunciator should be lit.

6. Replace the top cover. Disconnect the frequency standard input.

3.7.3 Procedure (TCXO Option)

Follow same procedure as in steps 1 through 4 and 6 above.

For step 5, adjust the TCXO frequency through a hole in the TCXO assembly and an aligned hole in the rear panel without removing the top cover.

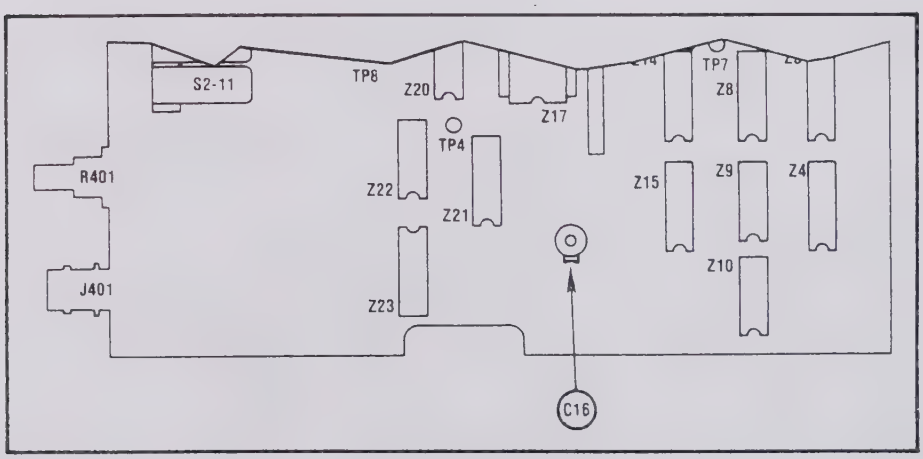


Figure 3-10. Location of Frequency Adjustment

4

PRINCIPLES OF OPERATION

4.1 SYSTEM BLOCK DIAGRAM

The Model 5845 is a multifunction counter programmed by front-panel (or optional remote signals) to measure and display frequency or period, to count discrete events, or to display time. As shown in the simplified block diagram of Figure 5-1, the major functional blocks that are configured for the different functions include:

Input Signal Conditioner (including selectable attenuator and filter)
Crystal-controlled oscillator and programmable time base
8-digit counter chain
Intercycle control counter
Multiplexed display

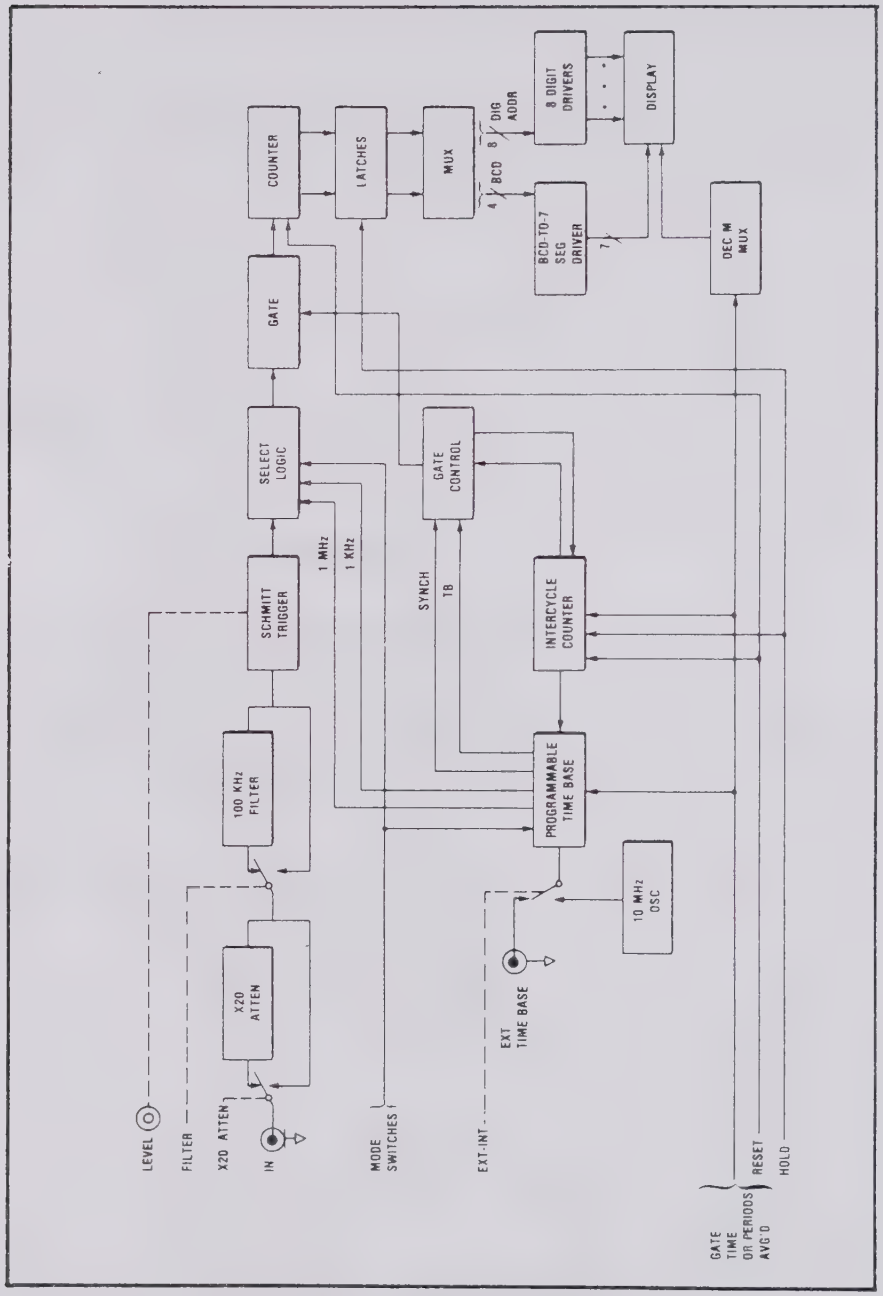


Figure 4-1. Block Diagram

In the **frequency measurement function**, the input signal is gated into the counter for a selected time period determined by the programmable time base. In response to the front-panel-selected **GATE TIME**, the gated input is counted for 0.01, 0.1, 1.0, or 10 seconds, and the display is made direct reading by automatic positioning of the decimal point corresponding to the selection.

In the **period measurement function**, the input signal is used to gate a precise 1 MHz time base into the counter chain. In response to the front-panel-selected **PERIODS AVGD**, the time base may be accumulated for 1, 10, 100, or 1000 periods between input signal peaks. The display is made direct reading by automatic positioning of the decimal point corresponding to the selection.

In the **time display function**, a precise 1 kHz time base is gated into the counter chain by the operation of the front-panel **TIME** pushbutton. The decimal point is positioned so that the display is direct reading in seconds with a resolution of 0.001 seconds.

In the **events measurement function**, the input signal is gated into the counter chain by the operation of the **EVENTS** front-panel pushbutton. The counter accumulates the number of input pulses, and the display is direct reading (no decimal point).

In both **TIME** and **EVENTS** measurements, the counters are permitted to run continuously, so that time in excess of 99,999.999 seconds, and events in excess of 99,999,999 (or multiples thereof) will be displayed, along with the appearance of the **OVERFLOW** annunciator lighted lamp.

The **Input Signal Conditioner** provides the impedance matching, selectable attenuation, selectable filter, and zero-crossing detection of the input signal. As indicated in Figure 4-1, this block also includes the **LEVEL** adjustment whereby the zero level band may be adjusted for low duty cycle measurements (see Chapter 3).

4.2 INPUT SIGNAL CONDITIONER

The function of the input signal conditioning is to develop square-wave trigger pulses from incoming signals. As shown in the simplified schematic of Figure 4-2, this is accomplished by a Schmitt trigger amplifier, after the incoming signal has been attenuated (optionally), filtered (optionally), clamped, and buffered.

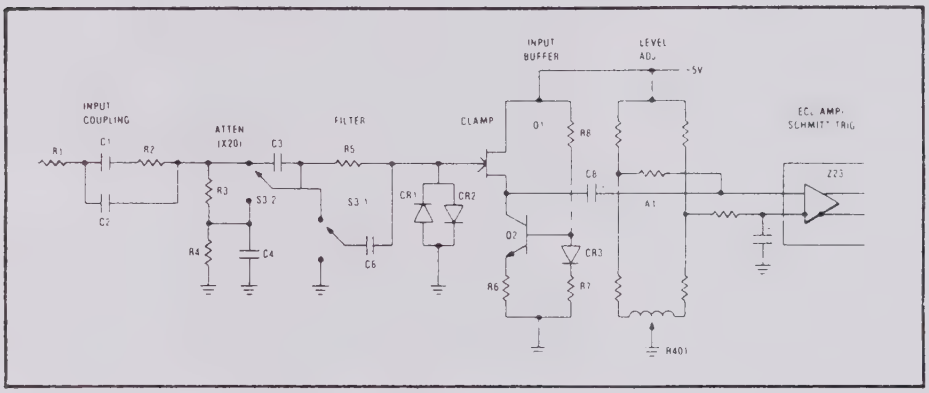


Figure 4-2. Input Signal Conditioner

The input is ac-coupled through C1, while R1 provides additional impedance matching to the coaxial input. The divider network consisting of R3 and R4 (C3 and C4) may be switched in by front-panel switch S3-2, and this introduces an attenuation of 20 over the specified frequency range. Capacitor C6 (43 pF) is switched in as a filter by front-panel switch S3-1, which, together with R5 (33K) constitute a single-pole low-pass filter with a 100 kHz cut off. Overload protection is provided by diode clamps CR1 and CR2 that limit the drive voltage to Q1, and by R2 and R5, that limit the current into CR1 and CR2. To prevent high frequency attenuation if the filter is not selected, C2 bypasses R2 and C6 bypasses R5.

Source follower Q1, biased by constant current sink Q2, buffers the input to the Schmitt trigger amplifier. The other input to the differential

trigger circuit is an adjustable level, determined by the front-panel control setting of R401. The front-panel control has a range of ±0.25 V, around the nominal +2.5 V common mode input to the Schmitt Trigger.

The Schmitt trigger amplifier shown in Figure 4-1 is part of integrated circuit Z23, which also contains a single decade counter. Outputs from Z23 are taken as ECL levels directly from the amplifer when in the period or events measurement functions, and as BCD-coded TTL levels from the decade counter in that chip when in the frequency measurement function.

4.3 PROGRAMMABLE TIME BASE

Figure 4-3 is a simplified block diagram of the chain of IC's that are used to develop the various timing control signals in the Model 5845. The master oscillator provides the basic 10 MHz signal that is counted down in Z14, Z13, Z4, and Z3. Z14 and Z13 are dual ÷10 counters, while Z3 and Z4 are dual programmable BCD count-down counters.

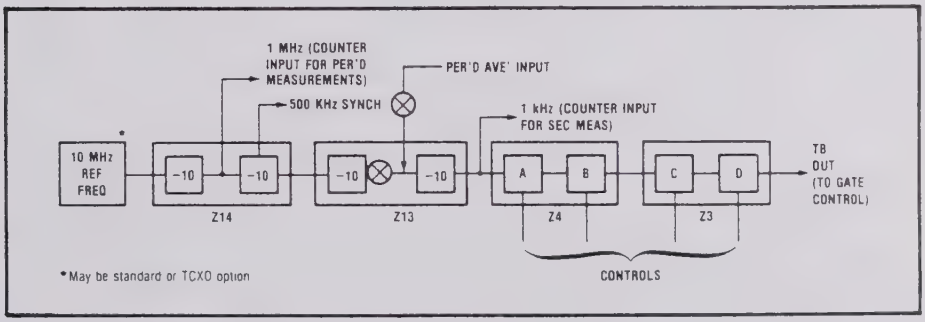


Figure 4-3. Programmable Time Base

As shown in the illustration, the 1 MHz signal for accumulating microseconds in the period measurement function is taken from Z14, after the first divide-by-10 action. It will be recalled from paragraph 4.1 that the gating of this time base is determined by the input signal, and portions of this time base chain are used to establish decade counter gating signals for the number of periods to be averaged.

A 500 kHz signal is taken from the first divide-by-2 step in the second half of the divide-by-10 components in Z14. This control signal is used as a synchronizing control to eliminate uncertainty in the start and stop of the count in the frequency measurement mode (refer to paragraph 4.4).

Input to Z13 is a 100 kHz signal (10 MHz ÷100). After the dual divide-by-ten in Z13, a 1 kHz signal is available to be used as the decade counter input when measuring time (in millisecond units).

The second ÷10 action of Z13 is used when in the period measurement function, and its output is passed to the count-down counters Z3 and Z4. This function is illustrated in simplified schematic in Figure 4-3.

Counters Z3 and Z4 are preset with a BCD value determined by the front-panel selection of **GATE TIME** or **PERIODS AVGD**. Each part of the dual counters may be independently preset with the BCD value **9** when a division by 10 is required, or by the value **0** when a unity division is required. Since there are four such dividers in series in the dual units (as shown in Figure 4-4), the series action can be programmed to provide a net division by 1, 10, 100, 1000, or 10 000 when required.

For example, in the measurement of frequency a gating period of 0.01 seconds requires a time base chain output at 100 Hz rate. Thus, a 1 kHz input to the chain requires only a division by 10 in one of the parts, and a division by 1 in the other three. Similarly, for the other gate times, additional ±10 factors are programmed to achieve the time base gating intervals.

For the averaging of periods, the decade counter gating is determined by the input signal itself (at the output of the Schmitt trigger after translation to TTL levels). When only a single period is to be measured, the gating control is made directly from the conditioned input without going through the time base chain shown in Figure 4-4. Therefore, the first requirement to count periods arises when **10** are selected at the front panel. The first divide-by-ten action on the input signal is performed in the latter part of the dual ÷10 counter Z13, as explained

previously, and the programmable counters must be preset for a net unity division (setting all parts to **0**). For 1000 periods to be averaged, these programmable counters need provide only two ÷ 10 actions in series, which, with the Z13 division, provides the required scaling.

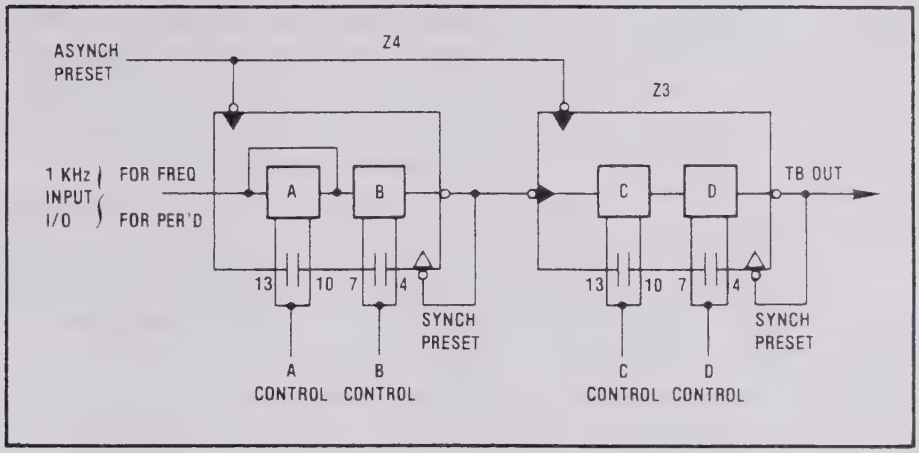


Figure 4-4. Simplified Schematic for Range Programming

Table 4-1 summarizes the programming presets established for the different front-panel selections.

Table 4-1
RANGE PROGRAMMING

CONDITION	A	B	C	D	÷ FACTOR	TB OUT FREQ
FREQ (0.01)	0	1	0	0	10	100 Hz
FREQ (0.1)	1	1	0	0	100	10 Hz
FREQ (1)	1	1	0	1	1000	1 Hz
FREQ (10)	1	1	1	1	10,000	0.1 Hz
PER'D (x1)	x	x	x	x	not used	not used
PER'D (x10)	0	0	0	0	1	IN/10
PER'D (x100)	0	0	0	1	10	(IN/10)/10
PER'D (x1000)	0	0	1	1	100	(IN/10)/100

4.4 GATE AND INTERCYCLE CONTROL

Gating the decade counter for measurement of frequency, period, events and the display of time is derived from the time base generation described in paragraph 4.3, above. Figure 4-5 is a simplified schematic of the circuitry used in the generation of the gating control signal. That illustration also includes the 6-state counter used for control of the actions in the ''intercycle'' period. Because the decade counter gating can be active only after the intercycle actions are completed, the two circuits are interdependent.

Refer to Figure 4-5; assume that the intercycle actions have just been completed, and that the time base has been enabled so that flip-flop Z9 is also enabled by the removal of the clear level. The first positive transition in the output of the time base waveform from Z3 (Figure 4-4) now

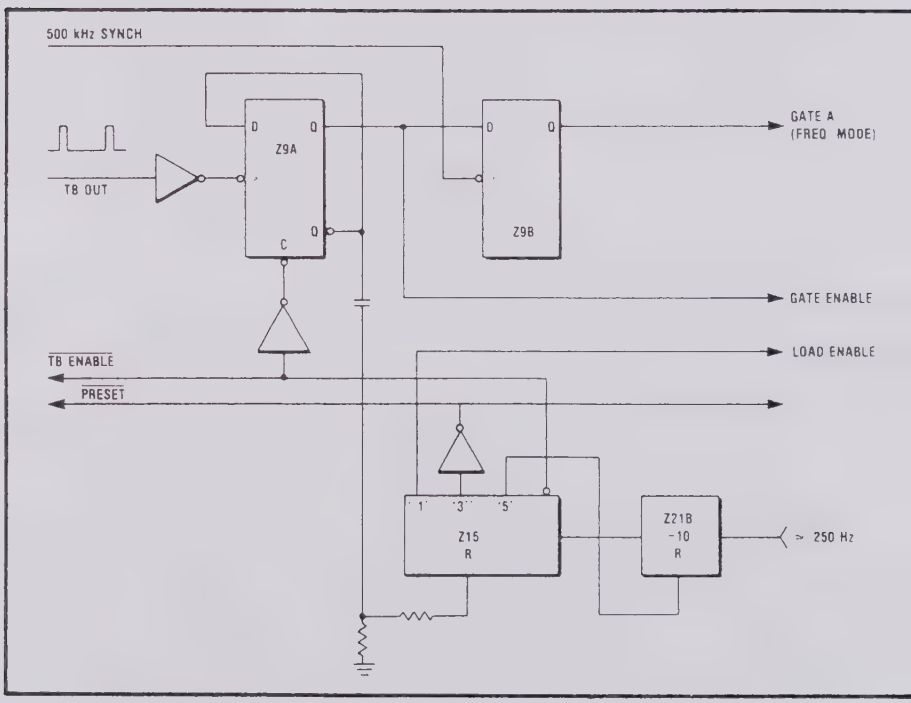


Figure 4-5. Gate Control and Intercycle Counter

clocks the flip-flop to produce a high-level Q output that enables the decade counting gate for the period, events, and time functions. The gate control is synchronized with a 500 kHz signal to produce the gating control for the frequency measurement function.

While the decade counting is enabled, State 5 disables Z21B, holding the intercycle counter Z15 in the sixth state. When the timebase input to Z9A next goes high, its transition clocks the negative level to the gating control signal and triggers the state counter to State 0.

The intercycle counter is advanced, as shown in Figure 4-5, by a clock signal of approximately 25 Hz, derived by a $\div 10$ of a 250 Hz signal. That 250 Hz signal is obtained from the digit scan control to be described later. Thus, the 6 states of Z15 are approximately 40 ms in duration. Of the 6 available states, only 3 are used. Control signals of 40 ms duration are used to latch the decade counter value, to preset the time base and reset the counters, and to return the intercycle counter to its reset state while, at the same time enabling the gate control flip-flop.

Figure 4-6 is a summary of the timing waveforms developed in the circuits described above and illustrated in Figure 4-5.

4.5 8-DECADE COUNTER & DISPLAY

The 8 decades of the measured value are instrumented in three sections: the six MSD values are developed in a single IC, Z17; the first decade (LSD) is either developed in the IC that contains the Schmitt trigger amplifier, Z23, or in a discrete decade counter driven by the output of the trigger (after proper level changes); the second decade is developed in a discrete counter. The 8-decade chain is illustrated in the simplified schematic of Figure 4-7.

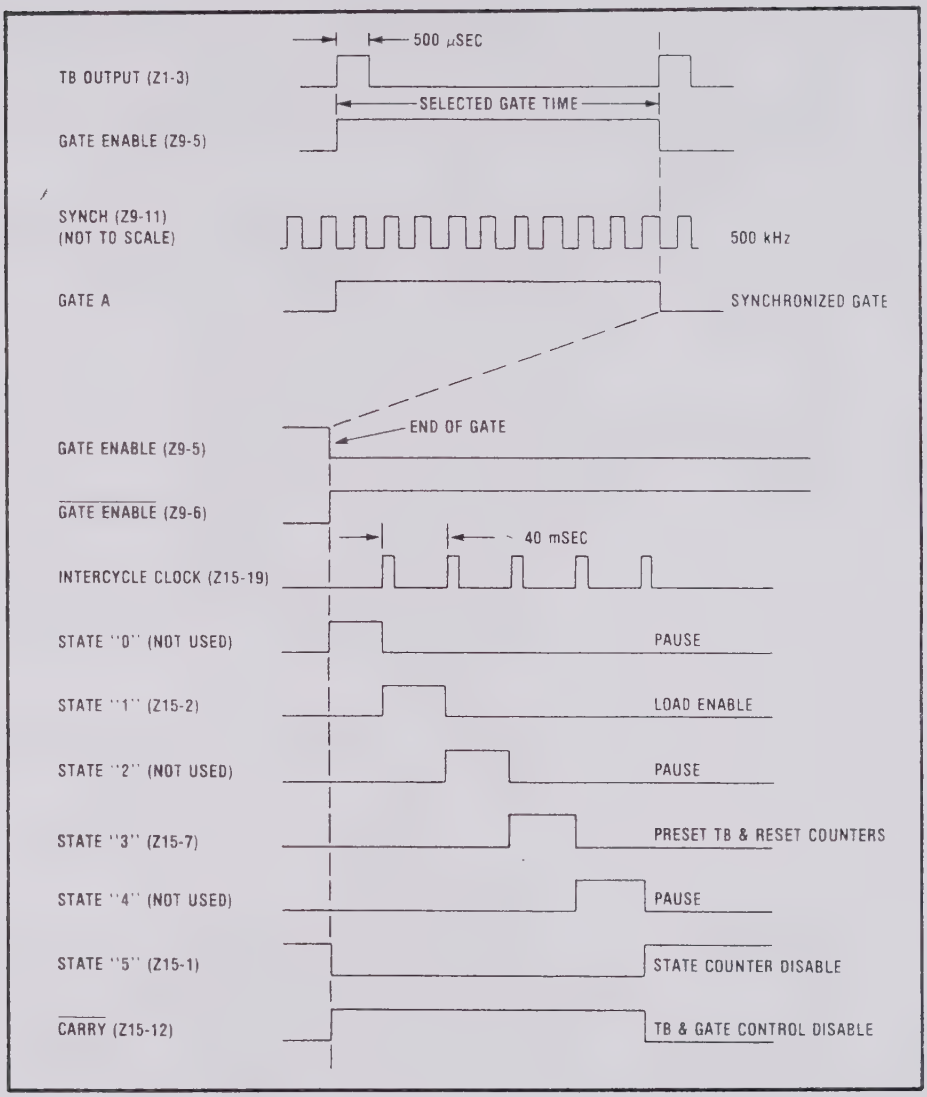


Figure 4-6. Timing Waveform Summary

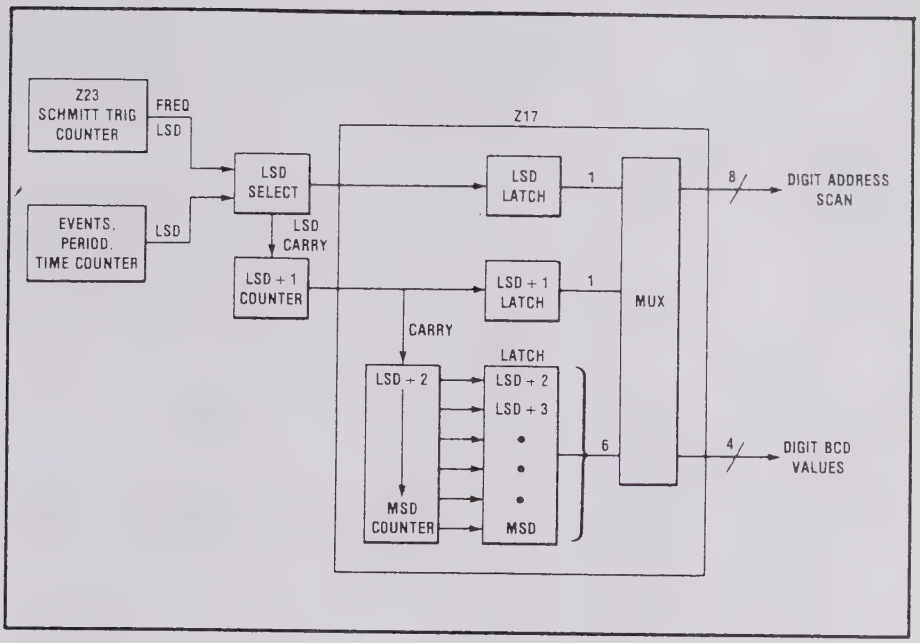


Figure 4-7. 8-Decade Counter Chain

As shown in the illustration, a single IC, Z17, is a multifunction component. It not only contains the counter chain for the 6 MSD values, but also contains the latches and multiplexers that store and transmit the values for the full 8 decades.

When in period or events measuring functions, the signal output is taken from the ECL Schmitt trigger amplifier and applied to the Q3, Q4 circuit to obtain a change to TTL levels. Previous paragraphs have described how the period input is used in the time base generation circuit. For events counting, the TTL signal is gated to counter Z21, whose BCD output is available at the input to Z20.

When in frequency measurement function, the signal output from the ECL Schmitt trigger is connected within Z23 to a single decade counter with TTL outputs in BCD format. This TTL signal is also available at another input port (4 lines) of Z20. Z20 is enabled to select either of these BCD inputs as the LSD counter value, and transmits them to Z17. The carry from the single-decade counter Z21 or from the internal counter in Z23 is then appropriately gated to Z19 to develop the BCD value of the second decade. Both decade values are transferred to Z17, where the internal elements complete the 8-decade chain.

At the end of the measurement gate, the 8 decade values are transferred to latches within Z17, replacing the values previously stored there. An internal cycle timer within Z17 multiplexes the 8 digit values as bit-parallel, byte series outputs on 4 lines, while the 8 digit address lines indicate which decade value appears at the output. One output line from Z17 indicates any overflow from the 8th digit.

The four BCD-coded output lines from Z17 are converted to 7-segment driver signals and connected to the display assembly where they are applied in parallel to the 8 digits. The digit address lines from Z17 are converted to separate digit drivers and connected to the digit cathodes in the display assembly. The counter overflow indication from Z17 is independently converted to a driver signal for the annunciator in the display.

Gate time signals and decimal point signals control individual drivers for the annunciators and decimal point in the display.

The digit address scan of Z17 is used, as explained earlier, to drive the intercycle counter. The digit scan is at an approximate 25 Hz rate for the full 8 decades, and the Model 5845 circuitry uses the addressing of digit 1 for the intercycle counting clock.

4.6 HOLD AND RESET FUNCTIONS

Front-panel pushbutton controls may hold the displayed value at any time. Operating the front-panel **HOLD** button disables all control gating to the decade counter and prevents the latched values currently in the display from being changed. When the I/O output option is installed, a low level **STOP** pulse signal is converted to a latched low level, and accomplishes the same result as the mechanically latched front panel pushbutton.

Releasing the front-panel **HOLD** pushbutton, returns the instrument to its counting function. When the I/O option is installed, applying a high level **START** pulse results in the resumption of the counter functions by removing the low level previously developed.

The 5845 may be reset to start a new counting cycle by operating the front-panel momentary-action **RESET** pushbutton. This resets the display counters to zero, and initiates the intercycle 6-state counter operation. When the I/O option is installed a low-level reset pulse may be applied at the edge connector terminal and accomplish the same action as for the front-panel switch operation.

4.7 FUNCTION AND RANGE SELECT SWITCHES

The four function switches **FREQ**, **PER'D**, **TIME**, and **EVENTS** are interlocked so that operation of any one automatically releases the previously operated selection. Since the operation is a break-before-make action, it is possible to leave all the switches in a nonoperative

state. This feature is used when the I/O option is installed, so that the switch action is essentially paralleled by electrical input control signals.

Each switch is a single-pole single-throw operation, connecting the +5 V supply to the control circuits when operated. In the off mode, the switch output is connected to digital ground by a 100 K pull-down resistor.

Front-panel switches for the selection of periods averaged or seconds of gate time are also interconnected with each other. They are single-pole single-throw components, and they are connected in the same manner as for the function select components.

Since the two groups of interlocked switches are mechanically independent subassemblies, either one or both groups may be left in the inoperative condition at the front panel (see above). As a result, it is possible to transfer control selectively for remote operation. That is, the function may be selected at the front-panel while the range is selected remotely. Or, the range may be selected at the front-panel while the function is selected remotely. Or, both range and function may be selected remotely.

It is also possible to introduce an external **time base oscillator** and to develop the frequency and period measurements in terms of the scale and accuracy of the external time base. Since the overall accuracy of the measurement of these functions is limited, in the main, to the accuracy of the time base oscillator, the user may wish to improve the instrument performance by supplying his own external oscillator. A rear-panel coaxial connector and selector switch are included in the option hardware so that the user may switch from internal to external time base at any time.

The 5845 may have been ordered with a temperature-compensated crystal oscillator assembly. This provides a more stable time base reference for accurate readings over extended periods and extended environments.

Remaining paragraphs of this chapter contain features of the design of the circuits that implement the functions noted in the block diagram. These descriptions are presented with reference to simplified schematics that are derived from the complete schematics bound in the rear of this manual. The simplified illustrations use the same reference symbols as employed in the complete schematic, but usually omit the peripheral circuitry, such as power supply connections, pull up resistors, by-pass capacitors, etc.

4.8 POWER SUPPLY

Refer to the reference drawing, D75-1023 for complete schematic of the power supply.

The input main supply is fused (F301) and RFI filtered (L1, L2, C24, C25) in the primary of power transformer T1. The transformer primary may be configured by internal connections for either 100, 115, or 230 Vac power sources. The transformer secondary output is full-wave rectified and develops the + 8 V supply for the display power. The rectified supply is applied to voltage regulator Z25 that develops a regulated + 5 V with respect to ground. This voltage supply powers all the digital logic (except for the display) and the analog signal conditioning circuits. Note that the return for the display power is displaced from the digital ground by CR8 so that the display power does not introduce transient disturbances into the digital logic circuitry.

4.8.1 Regulated and Unregulated Supplies

The power supply consists of a 5 V 3-terminal regulator (Z25) that provides +5 V with respect to earth ground. (See the reference schematic bound in the rear of this manual). This voltage is used to supply the analog signal conditioning and all the digital logic, except for the display circuit.

In addition to the regulated +5 V supply, an unregulated voltage, +8 V, is used to power the display. The display power, which can be as much as 400 mA, thus bypasses the regulator. The display current returns to the power supply at V^-, which is isolated from earth ground by a diode drop inserted in CR8, as shown in Figure 4-8.

4.8.2 Power-Up Resetting

Resetting of the 5845 counters is accomplished during normal operation by the operation of the front-panel **RESET** pushbutton, Switch S2-10, as shown in Figure 4-9. The resetting also is accomplished when first applying power, and this process is accomplished in the power supply circuitry, also illustrated in Figure 4-9.

When power is first applied, the +8 V rail comes up first (before obtaining regulated supply). This causes CR10 to conduct and to regulate the base voltage of Q5 at 3.9 V. Since the +5 V rail has not come up, Q5 is turned off, pulling the RESET line to ground through R30. As soon as the +5 V power becomes greater that 4.5 V, Q5 will turn on, and pull up the RESET line through R24.

This circuit also serves to reset the counters after a brief power loss, because Q5 responds quickly to pull down the RESET line and to keep it down until power is restored. Figure 4-10 summarizes the timing actions during the resetting operation of this circuit.

4.9 I/O OPTION

4.9.1 General

The I/O Option for the Model 5845 incorporates a number of distinct functions instrumented on a single field-installable pc-board. The option provides the user with:

Parallel BCD outputs, including decimal point location
Range and Function programmability or status

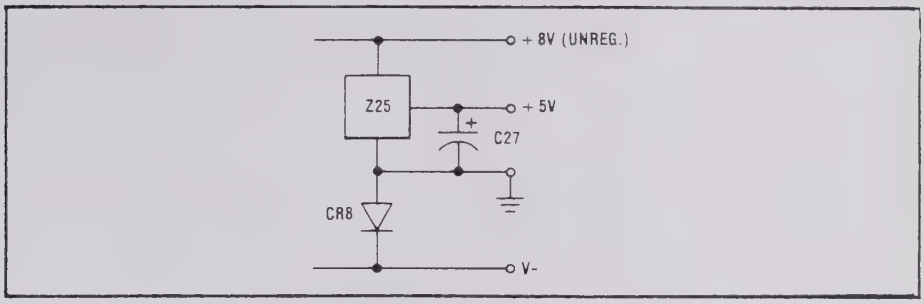


Figure 4-8. Isolated Returns of + 8V (Unregulated) and + 5V (Regulated) Supplies

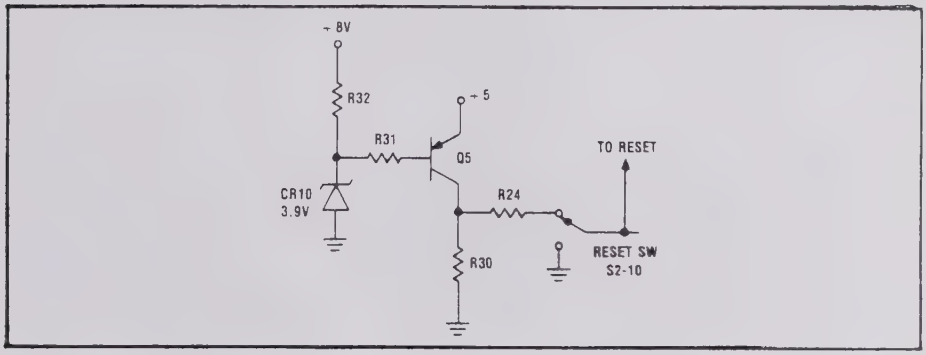


Figure 4-9. Power Up Reset Schematic

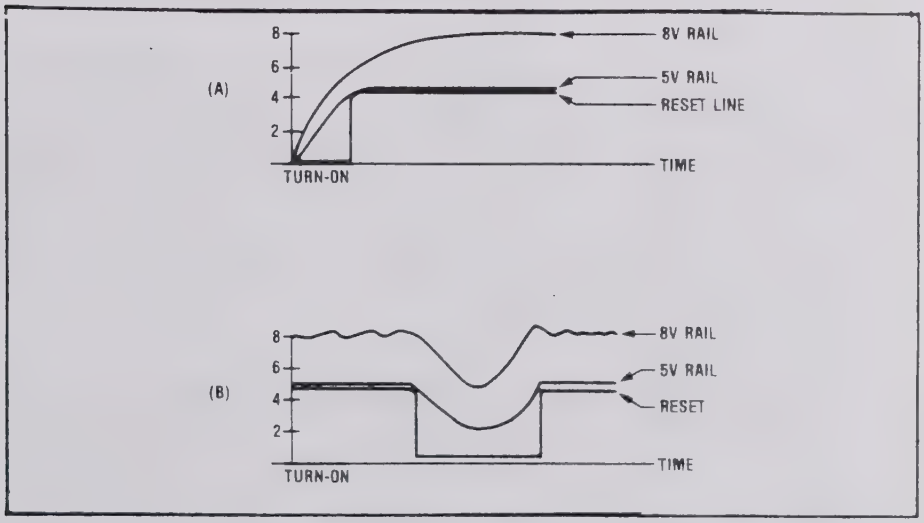


Figure 4-10. Timing Waveforms for Power Startup and Interrupt

Remote START, STOP, RESET capabilities, and
Provision for connecting an external reference frequency (time base) input.

Refer to the complete schematic of the I/O option, reproduced as part of the reference schematics at the rear of this manual.

4.9.2 BCD Outputs

As shown in the reference schematic, the bit-parallel digit-serial outputs of the main board (Z17) are essentially strobed into the 8-bit latches, Z202, Z203, Z204, and Z205 of the option board, so that 8 bits, representing the BCD values of 2 adjacent decades of the measurement, are stored in each latch. The user may then choose to transmit each bit on separate lines from the rear-panel connector, or to connect the BCD outputs as 8-bit bytes to a data bus. The capability to use this latter configuration is instrumented by providing an enable/disable line for each of the latches. When using the bus configuration, the user must address the appropriate latch for the decade pair.

4.9.3 Print Enable, Start, and Stop

The **PRINT ENABLE** signal goes low when the latches are being updated, and stays low for approximately 40 ms. Thus, the rising edge of this I/O output can be used to trigger an external printer when the output data will be valid. Note that the **PRINT ENABLE** stays low while counting TIME or EVENTS. Then, when the **HOLD** switch on the front panel, or the **STOP** signal via the rear panel, stops the count, the **PRINT ENABLE** line will rise to a high level, signalling the latching of the data values.

The **STOP** signal via the remote connection may be a low level pulse of minimal duration. It is processed in the 5845 to operate the hold circuits as for a depressed front-panel switch (for as long as desired) by using it to set a flip-flop circuit (Z206-4, -3). The flip-flop is then reset by the **START** signal.

5
MAINTENANCE

5.1 GENERAL

Model 5845 is a reliable, stable multifunction counter, designed for extended periods of trouble-free operation, and requiring minimum maintenance. Moreover, should an apparent malfunction be observed, 8 test points are optimally located on the main pc-board assembly to expedite trouble analysis

5.2 TROUBLESHOOTING STRATEGY

It is recommended that a ''positive'' troubleshooting procedure be used when diagnosing an apparent counter malfunction. In accordance with this procedure, one **confirms the proper performance of functional subdivisions** of the circuit. One can **always** deduce the proper performance with high confidence. But rarely can one be certain of the cause of improper performance. For example, if the input-to-output of an amplifier is observed to be within specifications, one may conclude that the amplifier is not the cause of any other malfunction observed in the system. In addition, one may also conclude that the power supply, at least for the levels required to sustain proper amplifier performance, is working properly.

On the other hand, if the input-to-output performance of the amplifier does not meet performance specifications, then the fault **may be** the result of a number of possible causes. The amplifier itself may be inoperative; the power supply may be marginally deficient (if otherwise apparently O.K.); the input loading may be defective; the output loading may be defective; the test setup may be defective, or the test instruments used to perform the test may be defective. And, in complex, multifunction circuits, the ''negative'' possibilities are almost boundless.

In keeping with the ''positive'' approach, the block diagram previously used in Chapter 4 has been reproduced with six of the test points located as shown in Figure 5-1. The remaining two test points are located in the power supply circuits. Table 5-1 defines each of the eight test points, and thereby indicates a probable use of that point in confirming ''positive'' performance.

Figure 5-2 defines a possible troubleshooting strategy that utilizes the test points in a well-defined sequence of actions to isolate the **GOOD** circuitry. The R/R (Replace or Repair) should be suggestive only, and not exhaustive in defining likely faulty components. Figure 5-2A covers the power and control timing circuitry, which can be checked by using the Model 5845 **TIME** function that does not include any external input (other than start and stop actions). Figure 5-2B covers the input signal conditioning and processing of circuitry.

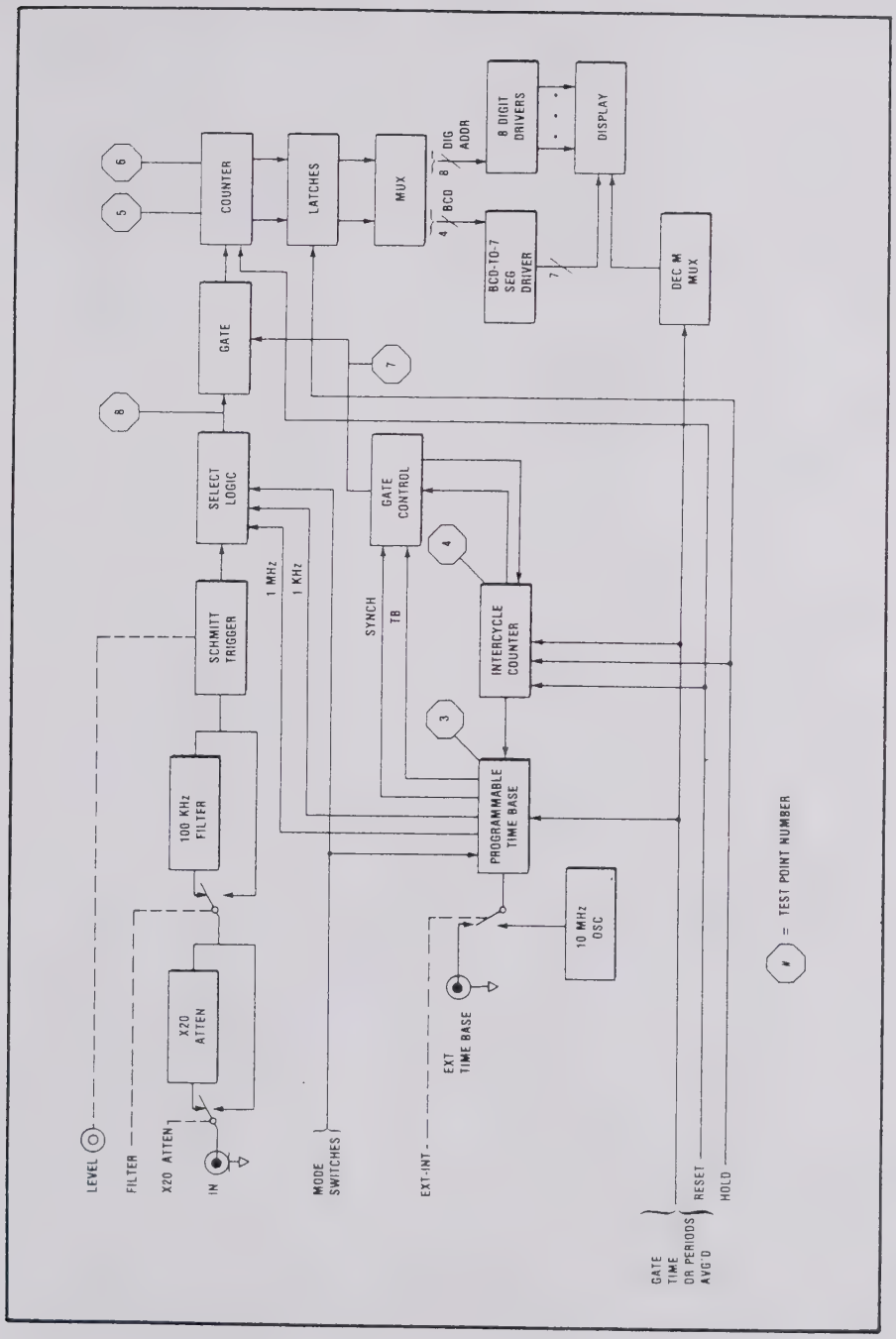


Figure 5-1. Test Point

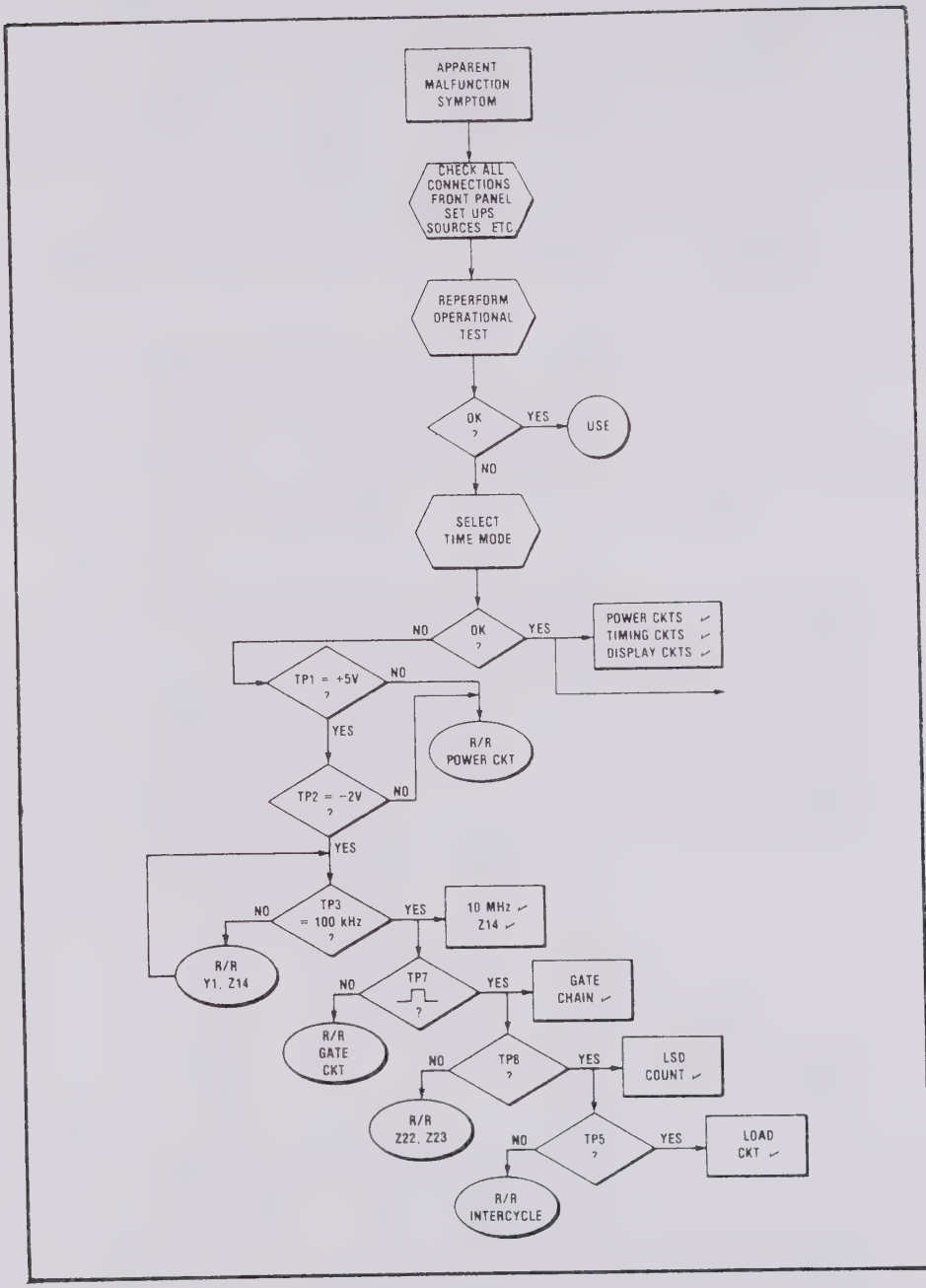


Figure 5-2A. Troubleshooting Flow Chart

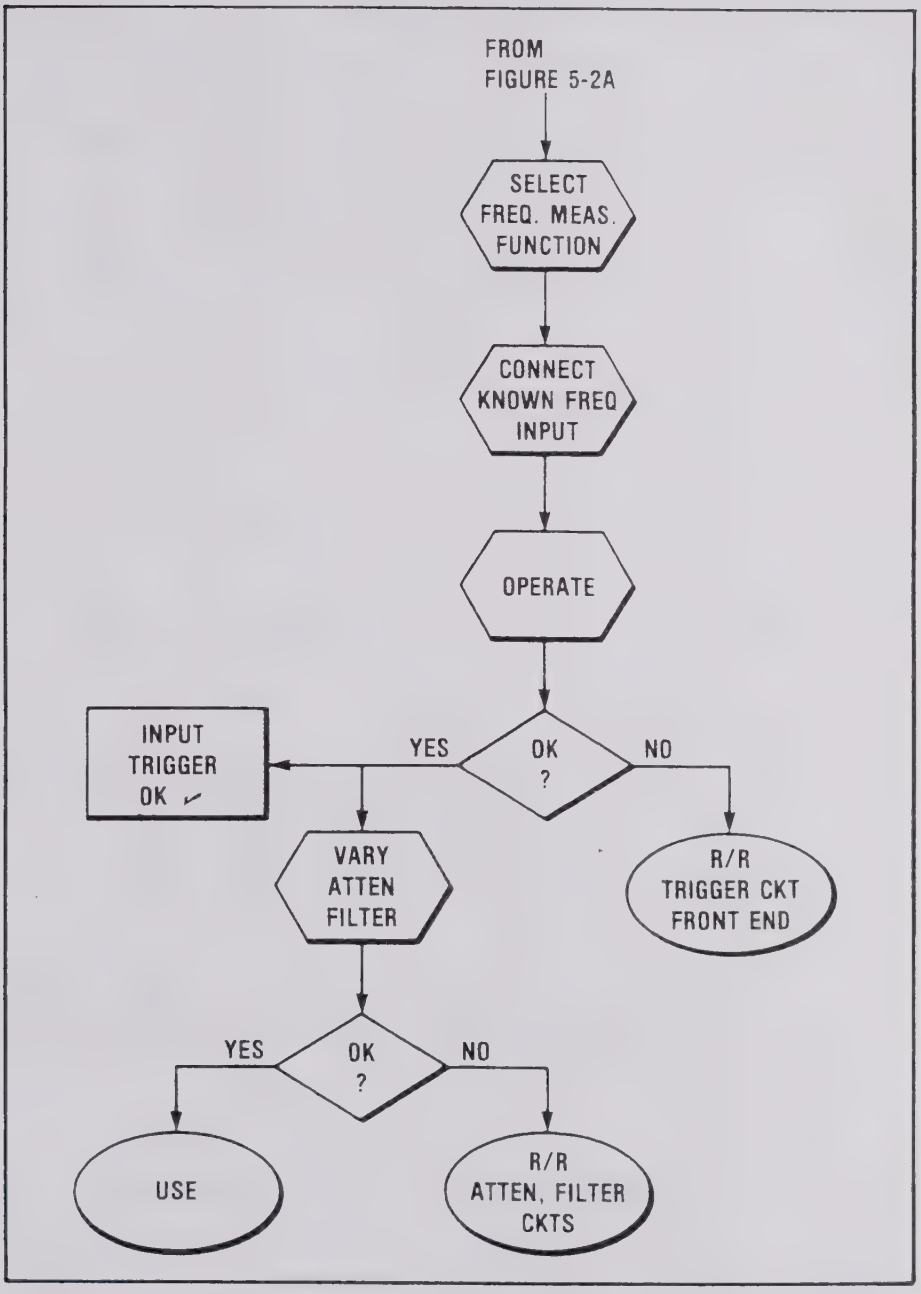


Figure 5-2B. Troubleshooting Flow Chart

5.3 TEST POINTS

Table 5-1
TEST POINTS

Number	Name	Comments/Maintenance-Assistance Information
1	+5 V	+5 V ±0.2 V (with respect to ground)
2	V–	–0.8 V ±0.25
3	100 kHz	Early part of clock countdown chain
4	Intercycle Clock	(From Z17 pin 2) ~ 200 Hz sequencing of multiplexer
5	Internal Load	LOAD ENABLE + TIME + EVENTS
6	Reset	Initializing counters
7	Gate Enable	Counter input control
8	LSD	First measurement decade

Table 5-1 lists the test points identified in the flow charts of Figure 5-2. Test point locations on the main pc-board assembly are shown in Figure 5-3. That illustration also shows the component location for appropriate repair and/or replacement.

Figure 5-4 illustrates the component locations for the I/O option board. Although there are no additional test points on that board, the I/O signal flow to the main board may be traced at the J201 to P1 connector for I/O to/from main board.

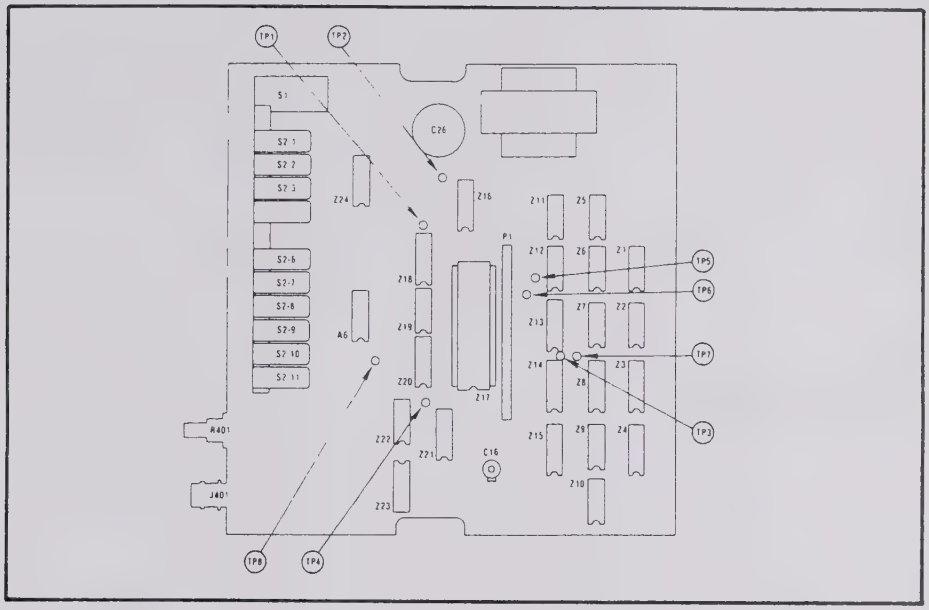


Figure 5-3. Test Points, Main PC Board

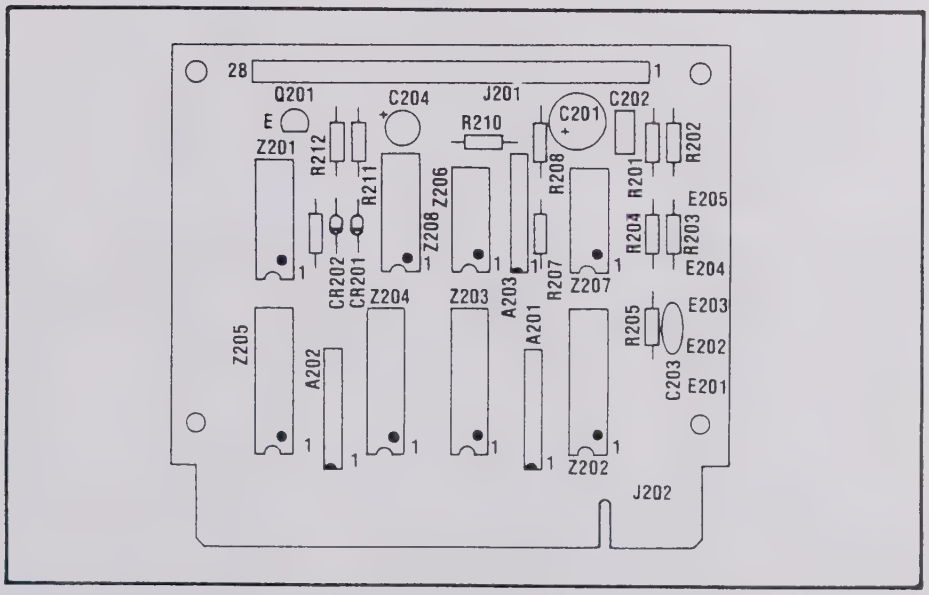


Figure 5-4. I/O Option PC Board

6
PARTS LISTS

6.1 GENERAL

Chapter 6 contains lists of replaceable electronic parts for Model 5845, including the I/O option board assembly. In particular, parts with symbol reference designations in the 0 to 99 series are installed on the main pc-board assembly, from 100 to 199 on the display assembly, from 200 to 299 on the option board assembly, from 300 to 399 on the rear panel assembly, and from 400 to 499 on the front panel assembly.

When ordering parts, please be sure to identify the part reference symbol designation and description, as well as the DP part number. In addition, identify the part number and **REVISION LETTER** of the pc-board.

6.2 STANDARD MODEL PARTS LIST

REFERENCE DESIGNATION	DESCRIPTION	PART NUMBER
A1	RES. NETWORK	22-78-1050
A2	RES. NETWORK	22-78-1051
A3, A4, A7	RES. NETWORK 2.2K, 5 RES, 6 PIN SIP	22-720000
A5	RES. NETWORK 100K, 7 RES, 8 PIN SIP	22-730004
A6	RES. NETWORK, 47Ω, 8 RES, 16 PIN DIP	22-711004
C1	CAPACITOR, .07μF, 250V, MYLAR	23-230012
C2	CAPACITOR, 150pF, 5%, DMN10	23-310027
C3	CAPACITOR, 10pF, 5%, DM10	23-310002
C4	CAPACITOR, 180pF, 10%, 200V, CERM	23-142002
C6	CAPACITOR, 43pF, 5%, DM10	23-310011
C7	CAPACITOR, .001μF,1KV, CERM	23-118202
C8, C10	CAPACITOR, 15μF, 10V, TANT	23-441003
C9	CAPACITOR, 47μF, 6.3V, TANT	23-441053
C11, C12, C23	CAPACITOR, .01μF, 150V, CERM	23-111006
C13, C24, C25	CAPACITOR, .005μF, 10%, CERM	23-118010
C14	CAPACITOR, 150pF, 5%, DM15	23-311015
C15	CAPACITOR, FSV, 5%, DM10	
C16	CAPACITOR, 2-9pF, TOP ADJ.	23-810023
C17, C18, C19	CAPACITOR, .1μF, 20%, 50V, MONO.	23-140062
C20	CAPACITOR, 0.47μF, 35V, 20%, TANT	23-441051
C21	CAPACITOR, 100pF, 10%, 1KV, CERM	23-111072
C5, 22, 28, 29	CAPACITOR, .1μF, 20%, 12V, CERM	23-118206
C26	CAPACITOR, 4700μF, AL. EL., 16V	23-620015
C27	CAPACITOR, 6.8μF, 20V MIN, TANT	23-441005
C30	CAPACITOR, 270pF, 10%, 1KV, CERM	23-110036
CR1,2	DIODE, SCHOTTKY, 5082-2800	24-110004
CR3, 4, 5, 11, 12	DIODE, IN4148	24-110001
CR6, 7, 8	DIODE, IN4004	24-104004
CR9	DIODE, IN270	24-140270
CR10	DIODE, IN7484, 3.9V	24-120066
CR13, 14	DIODE, A14U	24-102001
F301	FUSE, 3AG, 2/10 AMP, SLO-BLO	25-500004
DS101 - 108	DISPLAY, LED	25-227760

6.2 STANDARD MODEL PARTS LIST (Continued)

REFERENCE DESIGNATION	DESCRIPTION	PART NUMBER
J401	CONNECTOR, BNC,1094/U	25-340001
L1,2	INDUCTOR, 100μH	25-100101
Q1	TRANSISTOR, FET	24-78-1046
Q2	TRANSISTOR, MPS2369	24-232369
Q3, 4, 5	TRANSISTOR, MPS6519	24-246519
Q8 - Q15	TRANSISTOR, GES5818	24-235818A
Q16	TRANSISTOR, DARLINGTON MPSA13	24-230A13
Q6, Q7, Q17	TRANSISTOR, 2N3904	24-233904
R1	RESISTOR, 27Ω, 1/8W, 5%	22-012709
R2, R5	RESISTOR, 33K, 1/2W, 5%	22-033339
R3	RESISTOR, 910K, 1/4W, 5%	22-029149
R4	RESISTOR, 47K, 1/4W, 5%	22-024739
R6	RESISTOR, 75Ω, RN55D, 1%	22-3375R0
R7	RESISTOR, 604Ω, RN55D, 1%	22-336040
R8	RESISTOR, 3.74K, RN55D, 1%	22-333741
R9	RESISTOR, 10K, Y4W, 5% (OPT. F.S.V)	22-021039
R10	RESISTOR, 470Ω, 1/4W, 5%	22-024719
R11, 12	RESISTOR, 10Ω, 1/4W, 5%	22-021009
R17	RESISTOR, 130K, 1/4W, 5%	22-021349
R13, R19	RESISTOR, 22Ω, 1/4W, 5%	22-022209
R14, 22, 23, 32	RESISTOR, 1K, 1/4W, 5%	22-021029
R15	RESISTOR, 20K, 1/4W, 5%	22-022039
R16	RESISTOR, 2K, 1/4W, 5%	22-022029
R18,20,24,25,26 R30, R31, R33	RESISTOR, 22K, 1/4W, 5%	22-022239
R21	RESISTOR, 1M, 1/4W, 5%	22-021059
R27	RESISTOR, 100K, 1/4W, 5%	22-021049
R28	RESISTOR, 120Ω, 1/4W, 5%	22-021219
R29	RESISTOR, 10K, 1/4W, 5%	22-021039
R401	POTENTIOMETER, 500Ω	22-621001
R34	RESISTOR, 68Ω, 2W, 5%	22-056809
S1 & S2	POWER & RANGE/MODE SW (SCHADOW)	C78-1052
S3	ATTENUATOR/FILTER SW (SCHADOW)	C78-1053

6.2 STANDARD MODEL PARTS LIST (Continued)

REFERENCE DESIGNATION	DESCRIPTION	PART NUMBER
T1	TRANSFORMER	D78-1048
Y1	CRYSTAL, 10 MHz	B78-1001
Z1	IC 4001B	24-L04001
Z2,11	IC 4081B	24-L04081
Z3,4	IC 40102B	24-L40102
Z5,7	IC 4066B	24-L04066
Z6	IC 4075B	24-L04075
Z8	IC 4049	24-L04049
Z9	IC 74LS74	24-EOLS74
Z10	IC 74LS04	24-EOLS04
Z12	IC 4011B	24-L4011B
Z13,14	IC 74LS390	24-ELS390
Z15	IC 4017B	24-L04017
Z16	IC ULN-2003	24-330001
Z17	IC LS-7031 (LSI)	24-L07031
Z18	IC 74C48	24-G74C48
Z19	IC 74LS90	24-EOLS90
Z20	IC 4519B	24-L14519
Z21	IC 4518B	24-L14518
Z22	IC 74LS00	24-EOLS00
Z23	IC HI-SPEED FRONT END	24-78-1049
Z24	IC 4512B	24-L04512
Z25	VOLTAGE REGULATOR, 5V (LM342)	24-303425

6.3 I/O OPTION BOARD PARTS LIST

REFERENCE DESIGNATION	DESCRIPTION	PART NUMBER
A201 - 203	RES NETWORK, 22K, 4 RES, 8-pin SIP	22-731001
C201	CAPACITOR, 68 µF, 15V min, 20%	23-442004
C202	CAPACITOR, 68 pF, DM10	23-310019
C203	CAPACITOR, 0.01µF, 150V, CERM	23-111006
C204	CAPACITOR, 1µf, 35V, 20V	23-441001
CR201,202	DIODE, 1N4148	24-110001
J201	HEADER, STRAIGHT PIN	25-691005
J202	CONN. WITH KEY	25-300004
J203	CONN. BNC, UG1094/U	25-340001
Q201	TRANSISTOR, 2N3904	24-233904
R201	RESISTOR, 1.3K, ¼W, 5%, C	22-021329
R202	RESISTOR, 100Ω, ¼W, 5%, C	22-021019
R203	RESISTOR, 3.3K, ¼W, 5%, C	22-023329
R204	RESISTOR, 47K, ¼W, 5%, C	22-024739
R205	RESISTOR, 470Ω, ¼W, 5%, C	22-024719
R208	RESISTOR, 2.2K, ¼W, 5%,	22-022229
R209, 207, 210	RESISTOR, 22K, ¼W, 5%, C	22-022239
R211	RESISTOR, 33K, ¼W, 5%	22-023339
R212	RESISTOR, 10K, ¼W, 5%	22-021039
S201	SWITCH, TOGGLE, SPDT	25-451002
Z201	IC 4042B	24-L04042
Z202 - 205	IC 74C374	24-G74C374
Z206	IC 4001B	24-L04001
Z207	IC 74LS04	24-EOLS04-A
Z208	IC 80C97	24-G80C97

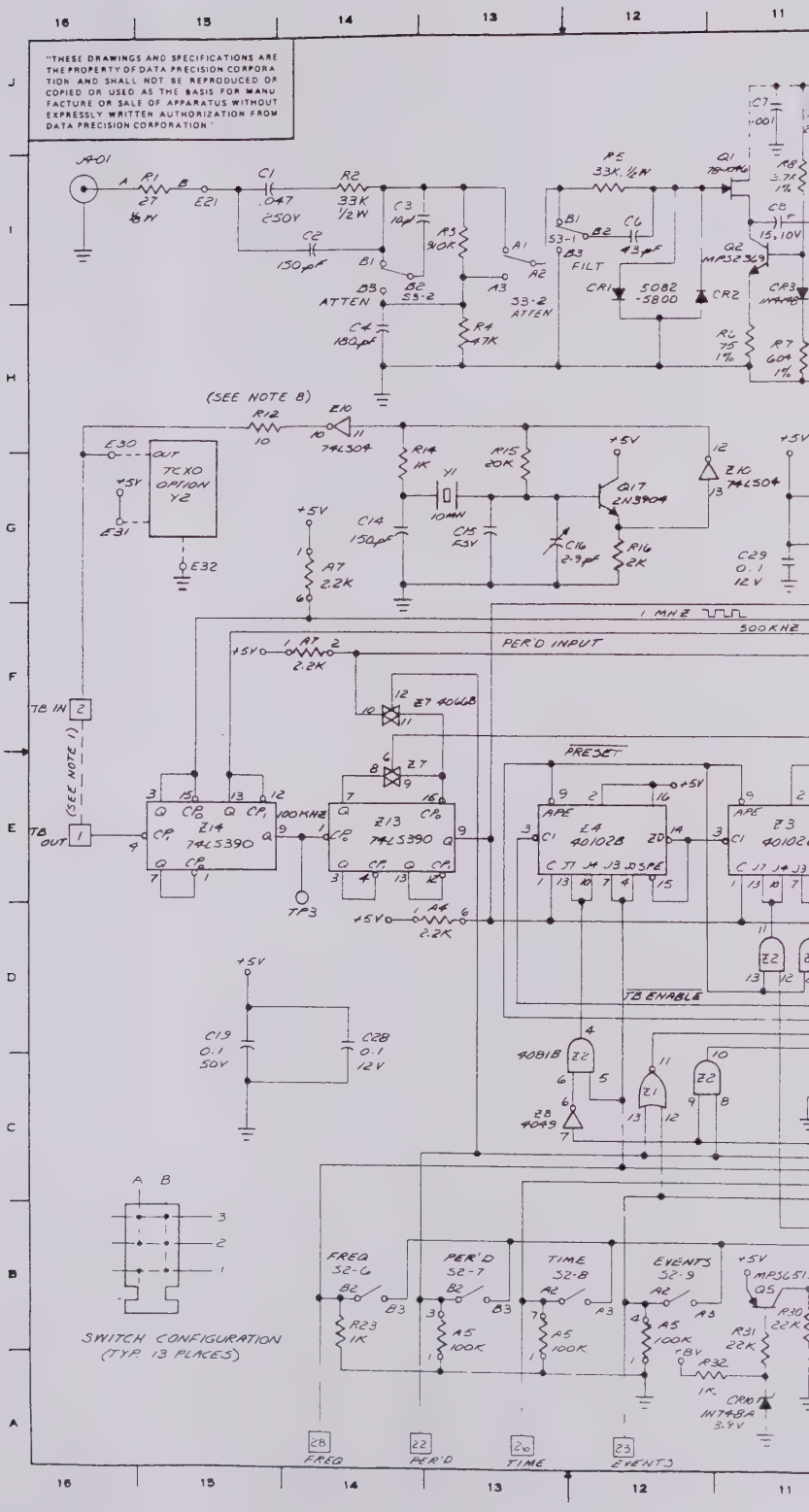
7
REFERENCE DRAWINGS

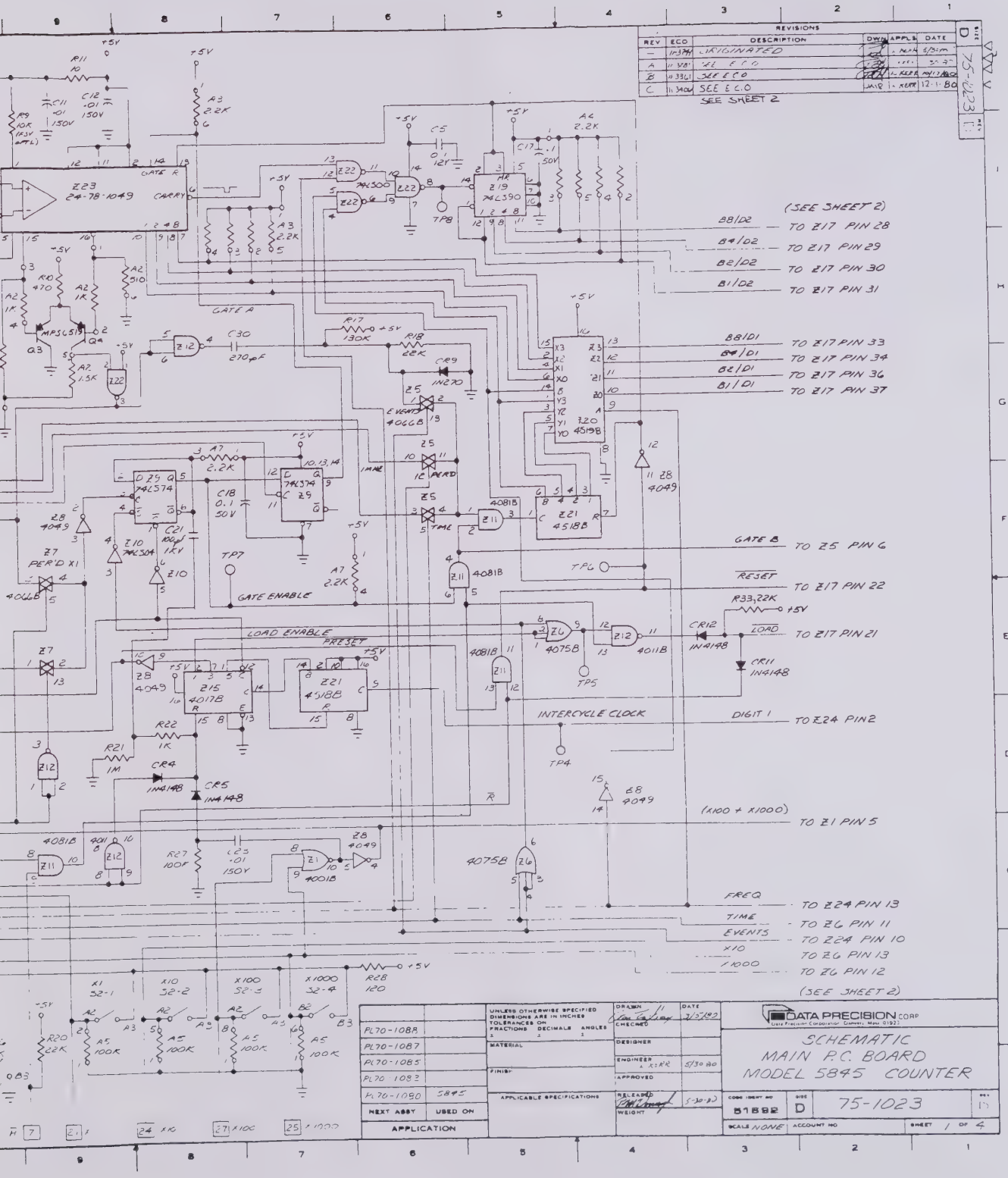
SCHEMATICS

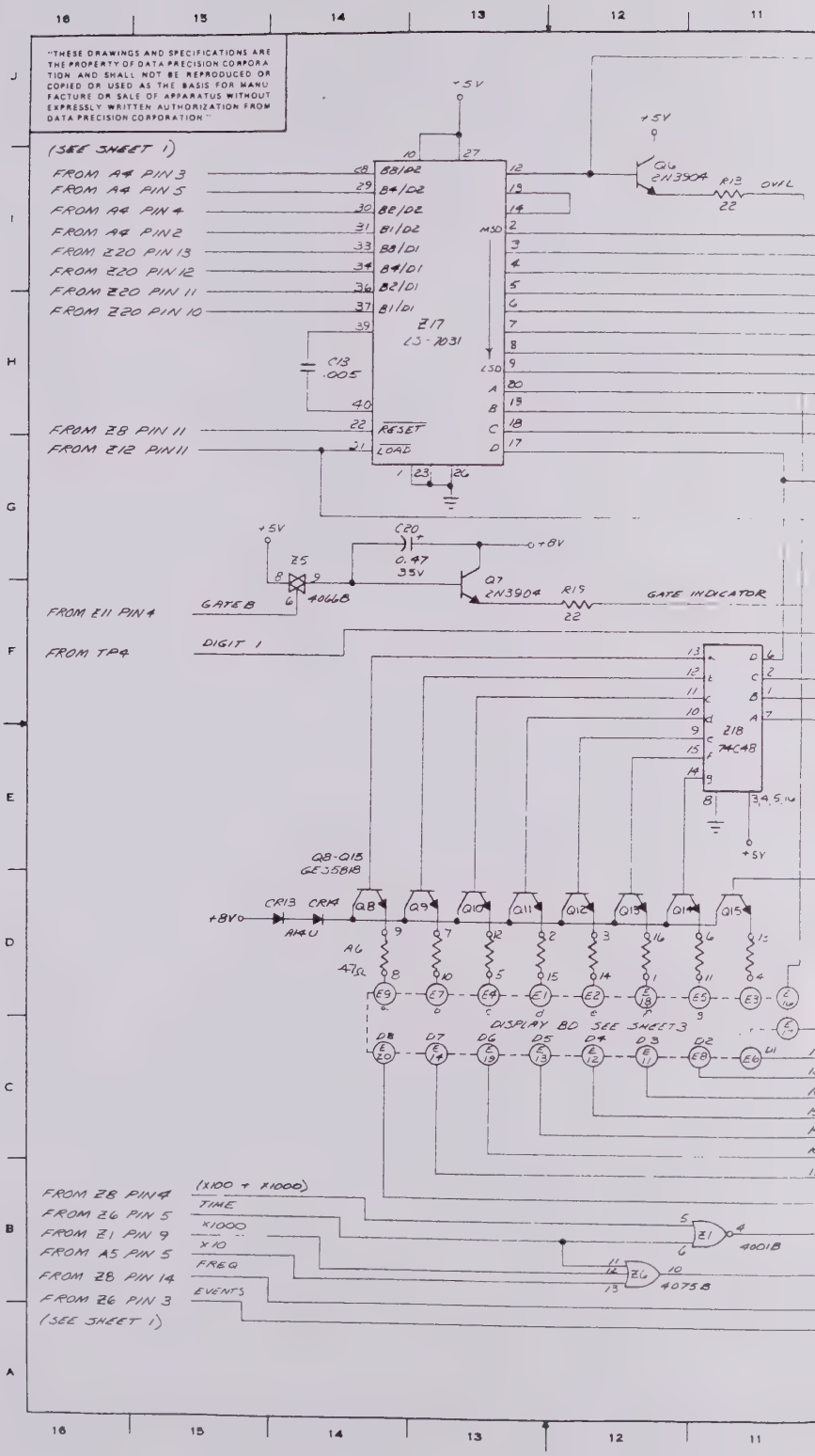
Main PC Board:	D75-1023 Sheets 1 and 2
Display Board:	D75-1023 Sheet 3
Input/Output Option:	D75-1023 Sheet 4

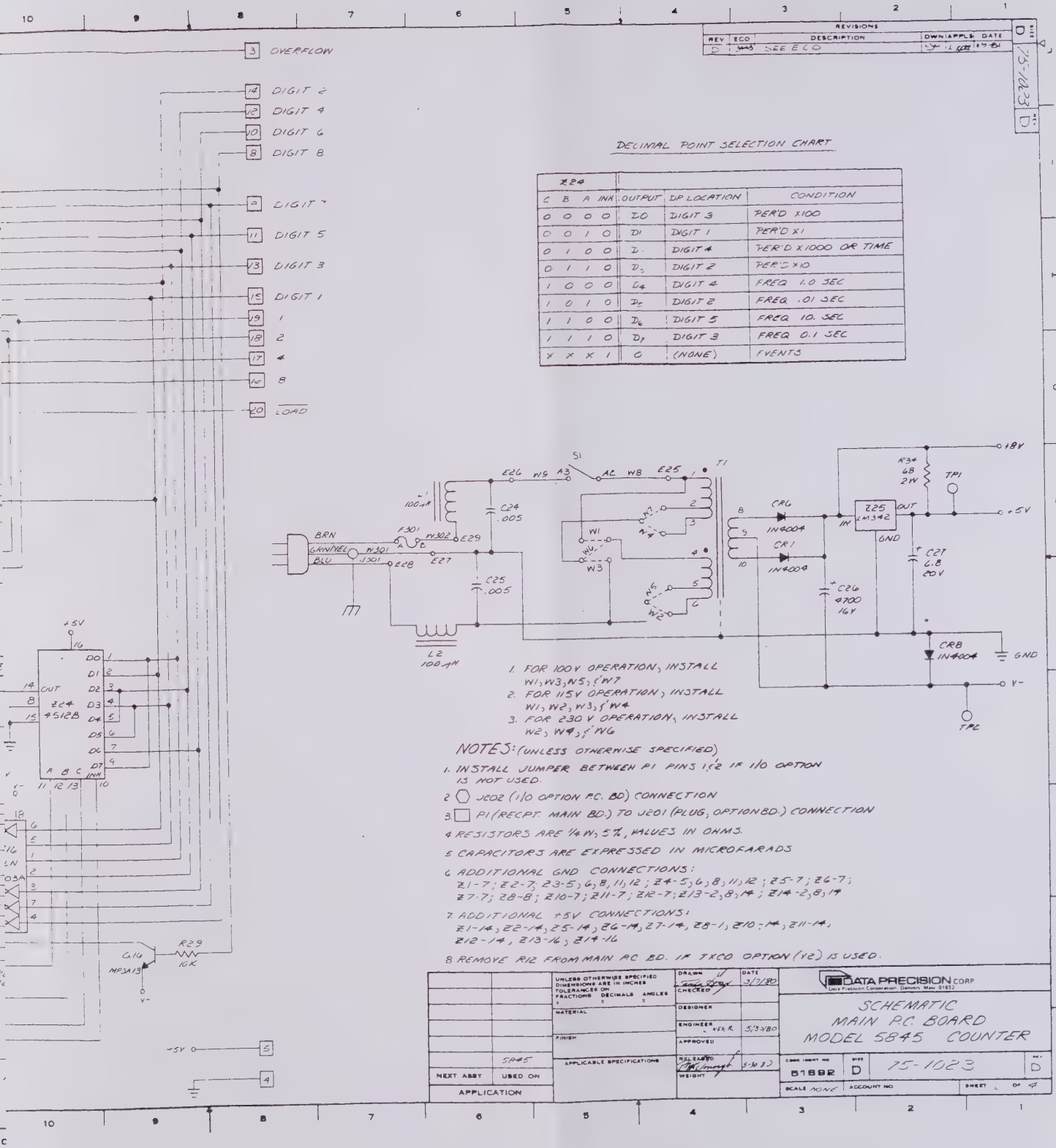
ASSEMBLIES

Main PC Board:	D77-1080
Display PC Board Assembly:	C77-1081
I/O Option Assembly:	C77-1082

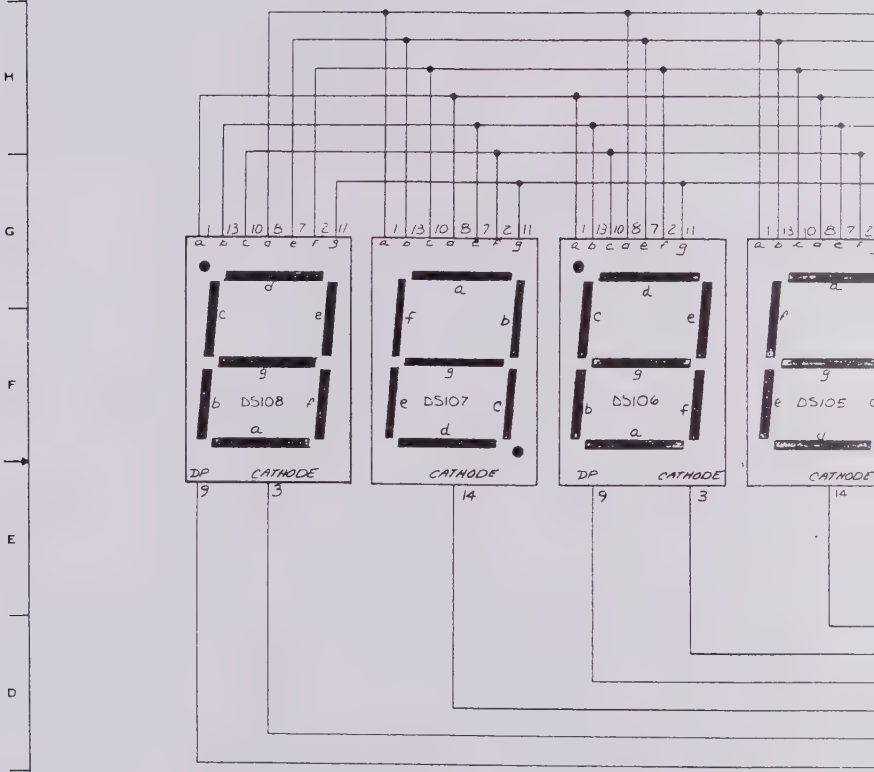

"THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF DATA PRECISION CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED AS THE BASIS FOR MANUFACTURE OR SALE OF APPARATUS WITHOUT EXPRESSLY WRITTEN AUTHORIZATION FROM DATA PRECISION CORPORATION."
J1-01
R1 27 1/8 W
C1 .047 250V
R2 33K 1/2 W
C2 150pf
C3 10pf
R3 340K
C4 180pf
R4 47K
ATTEN
33-2 ATTEN
FILT
R5 33K, 1/2 W
CR1 5082-5800
CR2
CR3
Q1
Q2 MPS2369
C6 43pf
C7 .001
C8 15, 10V
R6 3.7K 1%
R7 604 1%
R8 75 1%
(SEE NOTE 8)
R12 10
Z10 74LS04
E30
E31
E32
TCXO OPTION Y2
R14 1K
R15 20K
Y1 10MH
Q17 2N3904
C14 150pf
C15
C16 2-9pf
R16 2K
A7 2.2K
C29 0.1 12V
1 MHZ
500KHZ
PER'D INPUT
A7 2.2K
Z7 4066B
TB IN 2
(SEE NOTE 1)
TB OUT 1
Z14 74LS390
Z13 74LS390
100 MHZ
TP3
PRESET
APE
Z4 401028
Z3 401028
A4 2.2K
TB ENABLE
C19 0.1 50V
C28 0.1 12V
4081B
4049
SWITCH CONFIGURATION (TYP. 13 PLACES)
FREQ S2-6
PER'D S2-7
TIME S2-8
EVENTS S2-9
R23 1K
A5 100K
R30 22K
R31 22K
R32 1K
CR10 IN748A 3.4V
Q5 MPSL51
FREQ
PER'D
TIME
EVENTS

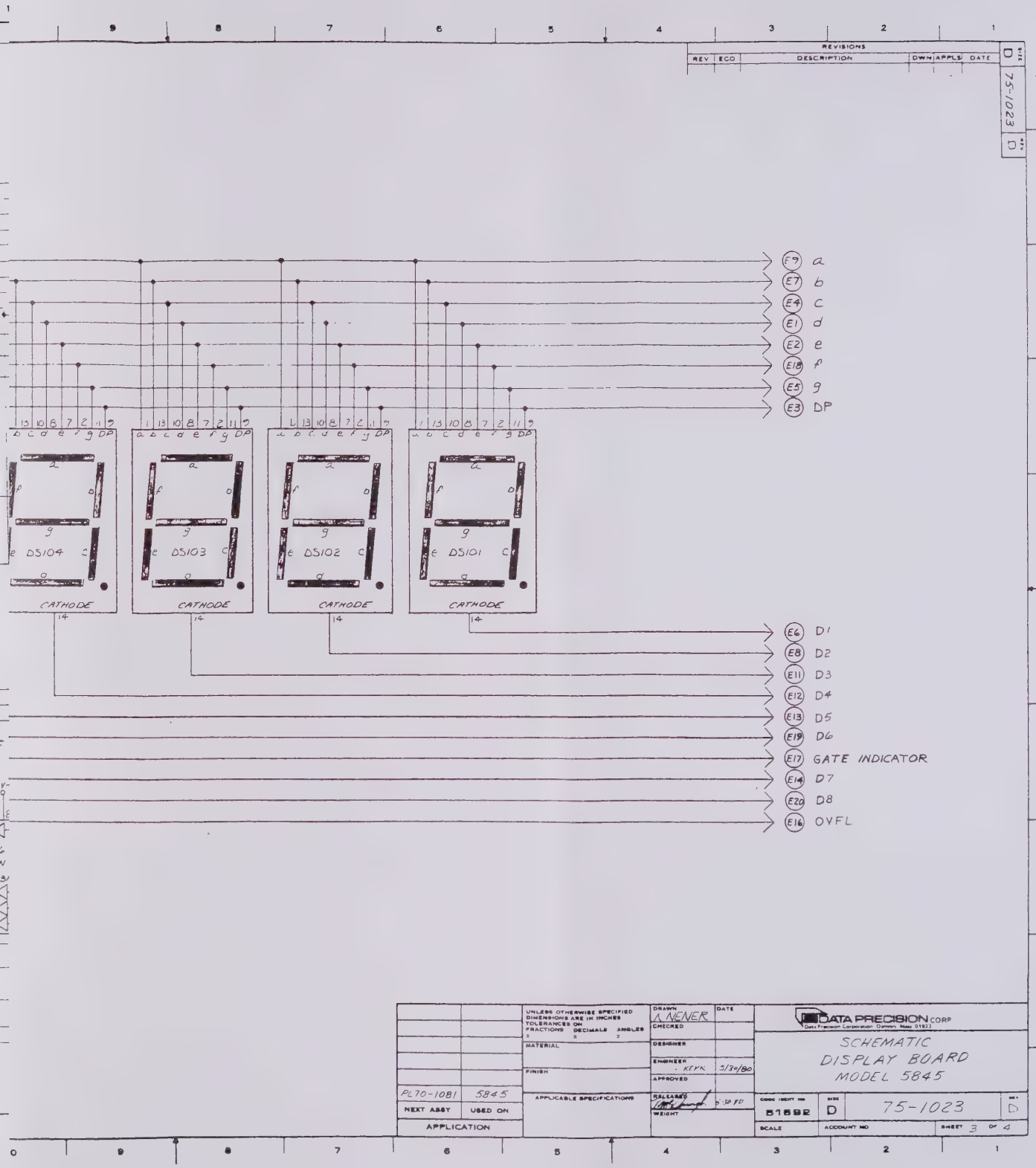

REVISIONS
REV ECO DESCRIPTION DWN APPR DATE
A 11-378 ORIGINATED
B 11-381 SEE E.C.O.
C 11-390 SEE E.C.O
SEE SHEET 2
Z23 24-78-1049 CARRY
GATE A
GATE B
Z22 74LS00
Z19 74LS390
Z20 45198
Z5 4066B
Z11 4081B
Z21 4518B
Z15 4017B
Z7 PER'D X1
Z10 74LS04
Z8 4049
Z6 4075B
Z24 4511B
Q3 MPS6519
Q4
CR9 IN270
CR12 IN4148
CR11 IN4148
CR4 IN4148
CR5 IN4148
TP7
TP6
TP5
TP4
TP8
GATE ENABLE
LOAD ENABLE
PRESET
INTERCYCLE CLOCK
EVENTS
TIME
LOAD
RESET
FREQ
(SEE SHEET 2)
BB/D2 — TO Z17 PIN 28
B4/D2 — TO Z17 PIN 29
B2/D2 — TO Z17 PIN 30
B1/D2 — TO Z17 PIN 31
BB/D1 — TO Z17 PIN 33
B4/D1 — TO Z17 PIN 34
B2/D1 — TO Z17 PIN 36
B1/D1 — TO Z17 PIN 37
GATE B — TO Z5 PIN 6
RESET — TO Z17 PIN 22
LOAD — TO Z17 PIN 21
DIGIT 1 — TO Z24 PIN 2
(X100 + X1000) — TO Z1 PIN 5
FREQ — TO Z24 PIN 13
TIME — TO Z6 PIN 11
EVENTS — TO Z24 PIN 10
X10 — TO Z6 PIN 13
X1000 — TO Z6 PIN 12
(SEE SHEET 2)
X1 32-1
X10 32-2
X100 32-3
X1000 32-4
PL70-1088
PL70-1087
PL70-1085
PL70-1083
PL70-1090 5845
NEXT ASSY USED ON
APPLICATION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
DRAWN 11/5/82
CHECKED
DESIGNER
ENGINEER 5/30/80
APPROVED
RELEASED 5-30-83
WEIGHT
DATA PRECISION CORP
SCHEMATIC
MAIN P.C. BOARD
MODEL 5845 COUNTER
CODE IDENT NO 81882
SIZE D
75-1023
SCALE NONE
ACCOUNT NO
SHEET 1 OF 4


"THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF DATA PRECISION CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED AS THE BASIS FOR MANUFACTURE OR SALE OF APPARATUS WITHOUT EXPRESSLY WRITTEN AUTHORIZATION FROM DATA PRECISION CORPORATION"
(SEE SHEET 1)
FROM A4 PIN 3
FROM A4 PIN 5
FROM A4 PIN 4
FROM A4 PIN 2
FROM Z20 PIN 13
FROM Z20 PIN 12
FROM Z20 PIN 11
FROM Z20 PIN 10
FROM Z8 PIN 11
FROM Z12 PIN 11
Z17
CJ-7031
C13
.005
C20
0.47
35V
+5V
+8V
Z5
4066B
Q7
2N3904
R15
22
GATE INDICATOR
GATE B
FROM Z11 PIN 4
FROM TP4
DIGIT 1
Q6
2N3904
R13
22
OVFL
Z18
74CA8
Q8-Q15
GE J5BIB
CR13
CR14
AHU
A6
47Ω
DISPLAY BD SEE SHEET 3
FROM Z8 PIN 4
FROM Z6 PIN 5
FROM Z1 PIN 9
FROM A5 PIN 5
FROM Z8 PIN 14
FROM Z6 PIN 3
(SEE SHEET 1)
(X100 + X1000)
TIME
X1000
X10
FREQ
EVENTS
Z1
4001B
Z6
4075B


REVISIONS
REV ECO DESCRIPTION DWN APPD DATE
D SEE ECO
75-1023 D
3 OVERFLOW
14 DIGIT 2
12 DIGIT 4
10 DIGIT 6
8 DIGIT 8
9 DIGIT 7
11 DIGIT 5
13 DIGIT 3
15 DIGIT 1
19 1
18 2
17 4
16 8
20 LOAD
DECIMAL POINT SELECTION CHART
Z24
C B A INH OUTPUT DP LOCATION CONDITION
0 0 0 0 D0 DIGIT 3 PER'D X100
0 0 1 0 D1 DIGIT 1 PER'D X1
0 1 0 0 D2 DIGIT 4 PER'D X1000 OR TIME
0 1 1 0 D3 DIGIT 2 PER'D X10
1 0 0 0 D4 DIGIT 4 FREQ 1.0 SEC
1 0 1 0 D5 DIGIT 2 FREQ .01 SEC
1 1 0 0 D6 DIGIT 5 FREQ 10. SEC
1 1 1 0 D7 DIGIT 3 FREQ 0.1 SEC
X X X 1 0 (NONE) EVENTS
S1
T1
E26 W9 A3
AC W8 E25
100-1A
C24 .005
C25 .005
F301
W302
E29
E28
E27
J301
W301
BRN
GRN/YEL
BLU
W1
W3
W2
W4
W5
W7
L2 100-1A
CR6 IN4004
CR1 IN4004
CR8 IN4004
+18V
R34 68 2W
TP1
Z25 LM342
IN OUT
GND
+5V
C27 6.8 20V
C26 4700 16V
GND
V-
TP2
1. FOR 100V OPERATION, INSTALL W1, W3, W5, & W7
2. FOR 115V OPERATION, INSTALL W1, W2, W3, & W4
3. FOR 230 V OPERATION, INSTALL W2, W4, & W6
+5V
Z24 4512B
D0 D1 D2 D3 D4 D5 D6 D7 INH
A B C
Q16 MPSA13
R29 10K
+5V
V-
NOTES: (UNLESS OTHERWISE SPECIFIED)
1. INSTALL JUMPER BETWEEN P1 PINS 1 & 2 IF I/O OPTION IS NOT USED.
2. ⬡ J202 (I/O OPTION P.C. BD) CONNECTION
3. ☐ P1 (RECPT. MAIN BD.) TO J201 (PLUG, OPTION BD.) CONNECTION
4. RESISTORS ARE 1/4 W, 5%, VALUES IN OHMS.
5. CAPACITORS ARE EXPRESSED IN MICROFARADS
6. ADDITIONAL GND CONNECTIONS:
Z1-7; Z2-7, 23-5, 6, 8, 11, 12; Z4-5, 6, 8, 11, 12; Z5-7; Z6-7; Z7-7; Z8-8; Z10-7; Z11-7; Z12-7; Z13-2, 8, 14; Z14-2, 8, 14
7. ADDITIONAL +5V CONNECTIONS:
Z1-14, Z2-14, Z5-14, Z6-14, Z7-14, Z8-1, Z10-14, Z11-14, Z12-14, Z13-16, Z14-16
8. REMOVE R12 FROM MAIN PC BD. IF TXCO OPTION (Y2) IS USED.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
DRAWN DATE 3/7/80
CHECKED
DESIGNER
ENGINEER 5/13/80
APPROVED
RELEASED 5/30/80
WEIGHT
DATA PRECISION CORP
SCHEMATIC
MAIN P.C. BOARD
MODEL 5845 COUNTER
CODE IDENT NO 51892
SIZE D
75-1023
REV D
SCALE NONE
ACCOUNT NO
SHEET 1 OF 4
5845
NEXT ASSY USED ON
APPLICATION

"THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF DATA PRECISION CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED AS THE BASIS FOR MANUFACTURE OR SALE OF APPARATUS WITHOUT EXPRESSLY WRITTEN AUTHORIZATION FROM DATA PRECISION CORPORATION."





PL70-1081	5845
NEXT ASSY	USED ON
APPLICATION	

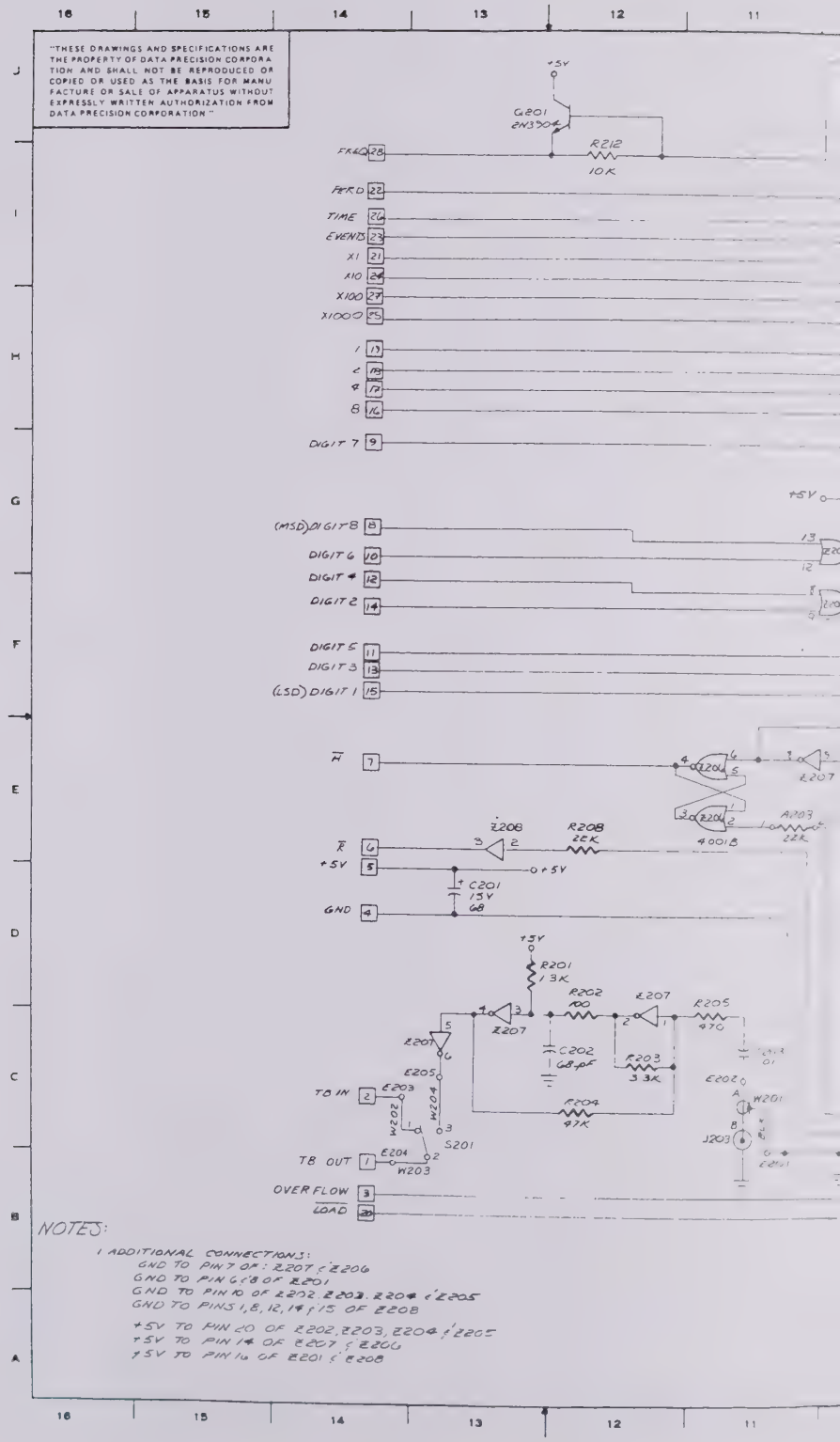
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

DRAWN K NENER DATE
CHECKED
DESIGNER
ENGINEER KEVK 5/30/80
APPROVED
RELEASED 5-30-80
WEIGHT

DATA PRECISION CORP
Data Precision Corporation, Danvers, Mass. 01923

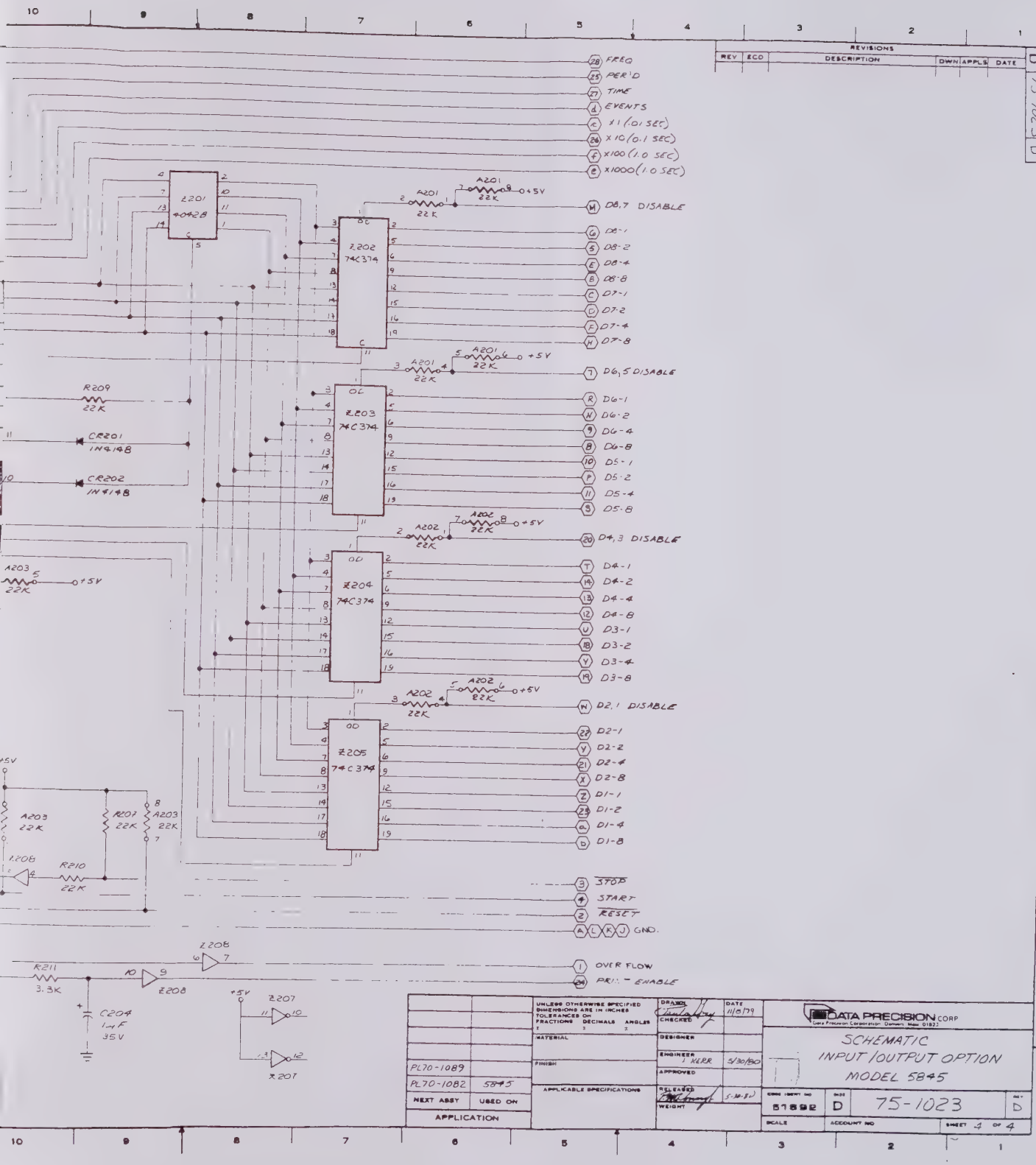
SCHEMATIC
DISPLAY BOARD
MODEL 5845

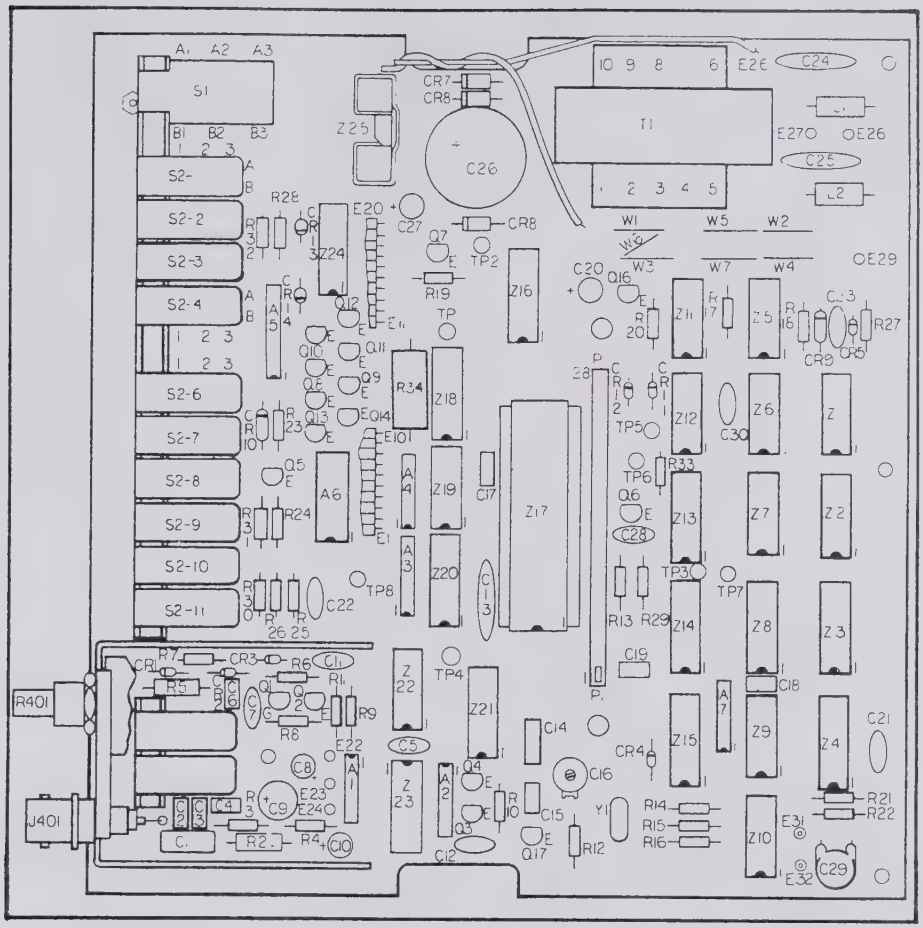
CODE IDENT NO 51592 | SIZE D | 75-1023 | REV D
SCALE | ACCOUNT NO | SHEET 3 OF 4



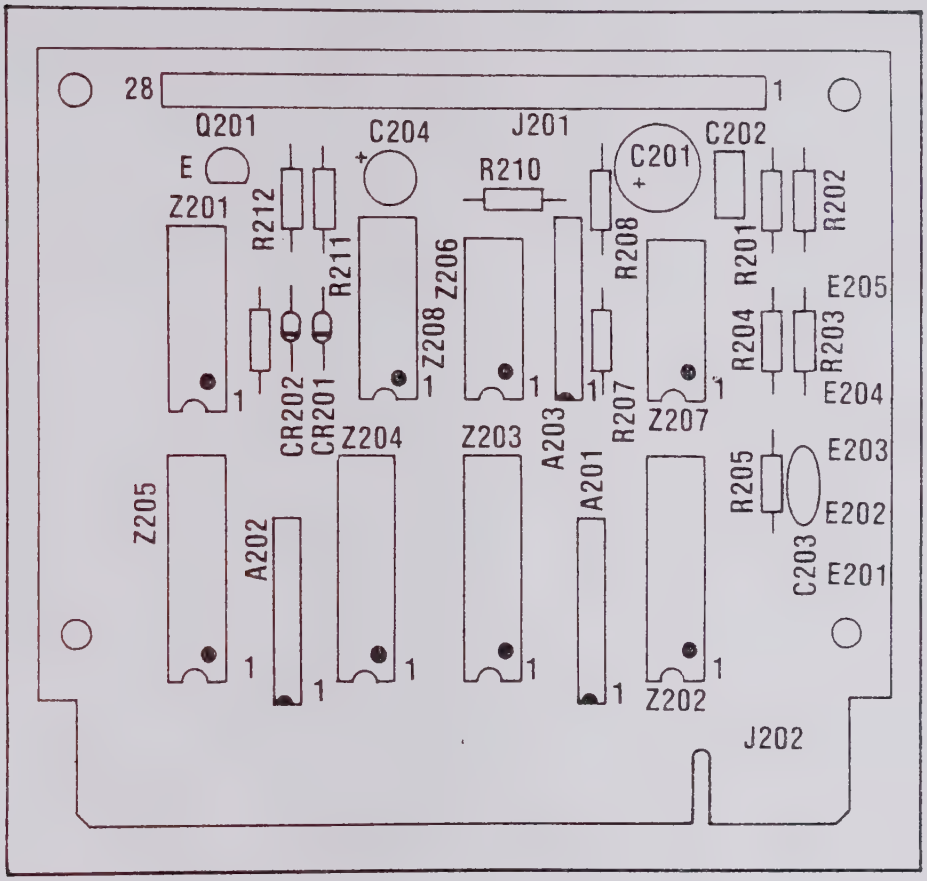
NOTES:

1. ADDITIONAL CONNECTIONS:
   - GND TO PIN 7 OF: Z207 & Z206
   - GND TO PIN 6 & 8 OF Z201
   - GND TO PIN 10 OF Z202, Z203, Z204 & Z205
   - GND TO PINS 1, 8, 12, 14 & 15 OF Z208
   - +5V TO PIN 20 OF Z202, Z203, Z204 & Z205
   - +5V TO PIN 14 OF Z207 & Z206
   - +5V TO PIN 16 OF Z201 & Z208


REVISIONS
REV | ECO | DESCRIPTION | DWN | APPL'D | DATE
SIZE D
75-1023 REV D
FREQ
PER'D
TIME
EVENTS
X1 (.01 SEC)
X10 (0.1 SEC)
X100 (1.0 SEC)
X1000 (1.0 SEC)
Z201 40428
A201 22K
+5V
D8,7 DISABLE
Z202 74C374
D8-1
D8-2
D8-4
D8-8
D7-1
D7-2
D7-4
D7-8
D6,5 DISABLE
R209 22K
CR201 IN4148
CR202 IN4148
Z203 74C374
D6-1
D6-2
D6-4
D6-8
D5-1
D5-2
D5-4
D5-8
A202 22K
D4,3 DISABLE
A203 22K
Z204 74C374
D4-1
D4-2
D4-4
D4-8
D3-1
D3-2
D3-4
D3-8
D2,1 DISABLE
Z205 74C374
D2-1
D2-2
D2-4
D2-8
D1-1
D1-2
D1-4
D1-8
R207 22K
Z206
R210 22K
STOP
START
RESET
GND.
Z208
R211 3.3K
OVER FLOW
PRINT ENABLE
C204 1uF 35V
Z207
X201
PL70-1089
PL70-1082 5845
NEXT ASSY
USED ON
APPLICATION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
DRAWN
CHECKED
DESIGNER
ENGINEER J. KERR 5/30/80
APPROVED
RELEASED 5-30-80
WEIGHT
DATE 11/6/79
DATA PRECISION CORP
Data Precision Corporation: Danvers, Mass 01923
SCHEMATIC
INPUT/OUTPUT OPTION
MODEL 5845
CODE IDENT NO 51892
SIZE D
75-1023
REV D
SCALE
ACCOUNT NO
SHEET 4 OF 4



Assembly, Main PC Board



Assembly, Option PC Board

72-1018-A

DATA PRECISION

Data Precision Corporation Electronics Avenue Danvers MA 01923

PRINTED IN THE U.S.A.